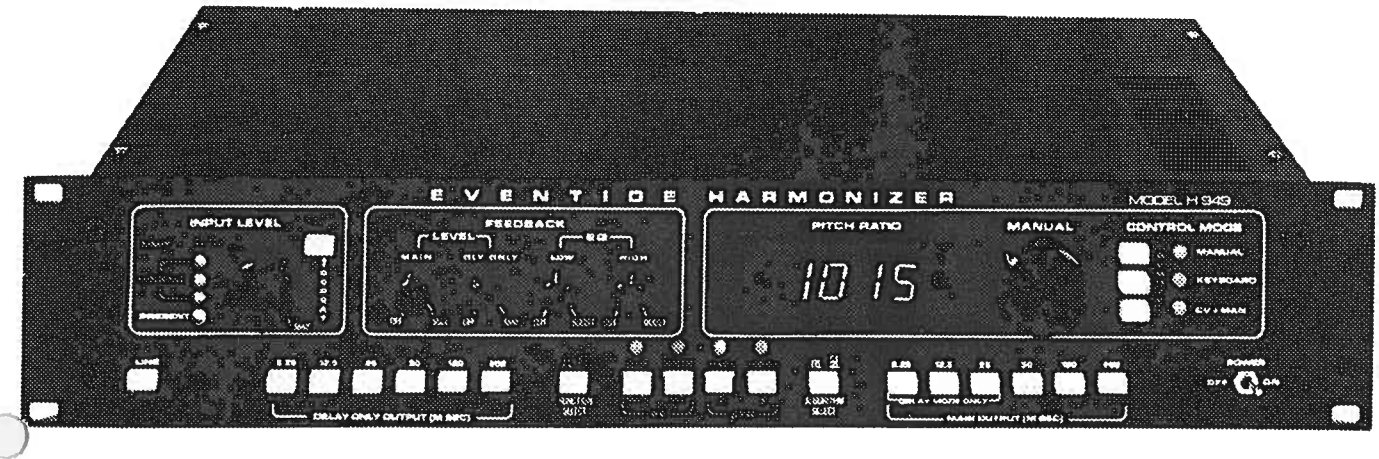
Eventide
the next step

H949
HARMONIZER®

INSTRUCTION MANUAL



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ALL RETURNED UNITS, IN OR OUT OF WARRANTY, MUST BE PREPAID TO OUR DOOR.

ALL RETURNED UNITS MUST BE ACCOMPANIED BY A COMPLETE TROUBLE REPORT, DETAILING ALL THE PROBLEMS EXPERIENCED, CONDITIONS OF OPERATION, ETC.

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REPLACEMENT OF PARTS UNDER WARRANTY will be done free of charge provided that the defective parts and the warranty card for the unit are received by Eventide.

EVENTIDE INC.

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DATE PURCHASED_____SERIAL NUMBER_____

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NAME OF PURCHASER_____

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SP2016 EFFECTS PROCESSOR/REVERB ( ) BD955 BROADCAST DELAY LINE ( )

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FL201 INSTANT FLANGER® ( ) 1745M AUDIO DELAY LINE ( )

* * * * *

IMPORTANT: YOU MUST FILL OUT THIS FORM TO ENSURE WARRANTY PROTECTION

AND MAIL WITHIN TEN DAYS OF PURCHASE TO:

EVENTIDE INC., 1 ALSAN WAY, LITTLE FERRY NJ 07643

MODEL H949 HARMONIZER
specifications:

INPUT CHARACTERISTICS	Impedance nominal 10 k, balanced, maximum level +24 dBm. Full dynamic range from −10 dBm to +24 dBm levels.
OUTPUT CHARACTERISTICS	Impedance nominal 150 ohms. Suitable for driving 600 ohms or greater at +18 dBm. Electronically balanced.
DISTORTION	Less than .15% at 1 kHz, reference output level.
DYNAMIC RANGE	Greater than 96 dB from clipping to noise floor.
PITCH VARIATION	1 octave up, 2 octaves down, continuously variable. Four-digit readout indicates precise ratio.
DELAY	Main output—in Pitch Change mode: 0 to 300 ms in 50 ms steps. In Delay mode: 0 to 393.75 ms in 6.25 ms steps. Delay Only output: 0 to 393.75 ms in 6.25 ms steps.
FREQUENCY RESPONSE	At any delay, unity pitch ratio: 20 Hz to 15 kHz, ± 1 dB. No degradation with increasing delay.
SIZE	Requires 8.89 cm (3½ ″) x 48.26 cm (19 ″) panel space. Extends 29.85 cm (11-¾ ″) behind panel.
POWER REQUIREMENTS	Switchable between 115 VAC (105–120 VAC), 50–60 Hz, and 230 VAC (220-240 VAC), 50–60 Hz. Nominal power dissipation 45 watts.
REMOTE CONTROL	Provision has been made for control by microcomputer using the IEEE standard interface bus (IEEE 488/1975). The HK940 keyboard can be used to control the pitch ratio in discrete musical steps. Option 05 mono keyboard controls one Harmonizer; option 06 polyphonic keyboard controls up to three Harmonizers. An input is provided to phase-lock the Harmonizer to any synthesizer. A 3 volt peak-to-peak signal is required. The pitch may be varied by a control voltage input in the 5 to 15 volt range (internally selected).

Harmonizer is the registered trademark of Eventide, Inc. for its audio pitch shifter special effects devices.

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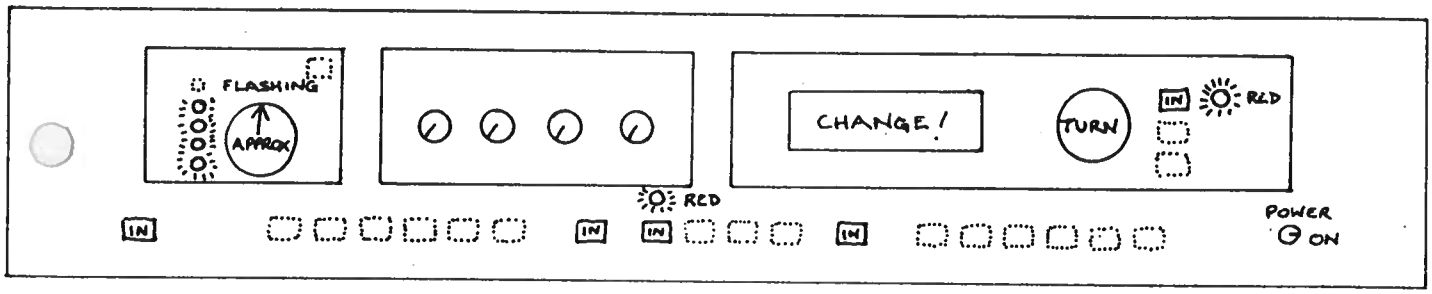
INTRODUCTION

The Eventide model H949 Harmonizer has a great many functions and modes of operation, which may seem confusing at first. We recommend that you spend some time familiarizing yourself with the different things the unit can do.

INSTALLATION — The H949 will operate best in a well-ventilated location. If the unit is going to be subject to vibration (when traveling, for example) we recommend some support for the rear of the unit, not just rack mounting.

LINE VOLTAGE — See section below. It is very easy to change the H949 from 115 to 230 volts. Remember that while applying 115 volts to a unit set for 230 will not hurt it (it won't work, though), applying 230 volts to a unit set for 115 may well prove disastrous. Check again when the unit goes along on your world tour.

CONNECTION — The Harmonizer needs to be supplied with line level - if you are feeding it from a microphone, guitar, or similar, you will need a pre-amp. Connect the AC power cord, the input and output connectors, then set the front panel controls as shown below. This is a simple setting which will enable you to change the pitch of the input signal by turning the MANUAL knob. After that - experiment!



CONTROL DESCRIPTION

This section describes the various operating controls and front panel indicators of the Harmonizer model H949. Because of the large number of operating modes, many of the controls have multiple functions, and interact in unexpected ways. To avoid multiple cross references, the multimode controls may be partially described under more than one heading. Please be sure to read and understand the operation of all the operating controls before using the Harmonizer.

POWER ON/OFF

CAUTION: Before operating this control, be sure that the Harmonizer is set to the AC power line voltage appropriate for your location. As detailed in the Specifications, the 949 will operate at 115 VAC (105 - 120 VAC) and 230 VAC (220 - 240 VAC). If your local line voltage is consistently lower than these ranges, a step-up transformer may be necessary. If your local power line is subject to significant fluctuations, it will be advisable to use a voltage regulating transformer.

The POWER control applies AC power to the Harmonizer. No power is consumed when in the OFF position.

LINE IN/OUT

This control switches the Harmonizer IN and OUT of the audio circuit to which it is connected. When the control is IN (physically depressed), the Harmonizer INPUT is connected to the internal circuitry, and the two OUTPUTS are connected to their respective output amplifiers. When the switch is OUT the Harmonizer INPUT is directly connected to the two OUTPUT jacks and all the Harmonizer circuitry is bypassed.

Note that in the OUT position power need not be applied to the unit for signal to pass through. This is a useful diagnostic tool if a malfunction is suspected. If no signal is heard in the OUT position, it is almost certainly caused by defective external wiring.

INPUT LEVEL CONTROL AND INDICATOR GROUP

The INPUT LEVEL control is used to set the optimum operating level for the Harmonizer. The control operates as a conventional "volume" control, increasing signal level as it is rotated further clockwise.

The LEVEL INDICATOR GROUP of 5 Light Emitting Diodes (LED's) provides a visual cue as to the whether the LEVEL control is set correctly. The lowest, yellow LED indicates that a signal is being applied to the input. It comes on at approximately 40dB below clipping. The three green NORMAL LED's become illuminated at various levels below clipping, and indicate that a proper driving signal is present at the Harmonizer input. The red LIMIT indicator becomes illuminated within 1dB of clipping, and indicates that the input signal has instantaneously exceeded the clipping threshold. Note that all of these indicators are peak responsive, and will light on "peaky" material even though the average signal level may be quite low.

The INPUT LEVEL control should ideally be set at a point where the input signal drives all three green LED's, but never flashes the LIMIT indicator.

REPEAT CONTROL

This locking push button control is used to CAPTURE and REPEAT the data stored in the Harmonizer's digital memory. It is included in the INPUT control block because it, in effect, cuts off the external input signal and supplies an internal one instead. Depressing the control causes all data in the memory to remain and recirculate indefinitely, either until the REPEAT mode is exited, or power turned off.

When in the REPEAT mode, the action of the LEVEL INDICATOR LED's is reversed, so that as the input signal amplitude increases, the LED's become progressively extinguished. This provides a continuing indication of the input signal level while reminding the user that the REPEAT mode is in effect and the actual signal input is being disregarded.

When attempting to "capture" a particular signal segment with the REPEAT control, remember that the signal segment captured is that which is present in the memory at the instant the switch is depressed. If you are listening to a delayed output, part or all of the signal segment you heard immediately prior to depressing the control will be lost, depending upon the delay setting. For this reason, one should monitor either the input signal, or an undelayed output when attempting to capture specific words or segments.

FEEDBACK CONTROL GROUP

This group of controls routes a portion of the two output signals back to the input amplifier. The output of this group mixes with the signal obtained from the INPUT jack, but is independent of the gain adjustment provided by the INPUT LEVEL control. The gains are normalized so that with EQ controls approximately centered, the feedback level varies from 0 to 100% (loop gain of unity or "infinite" sustain) as either of the LEVEL controls is varied from OFF to MAX. The individual controls work as follows:

The MAIN LEVEL control adjusts the feedback from the MAIN (pitch change/effect) output to the input.

The DLY ONLY LEVEL control adjusts the feedback from the DELAY ONLY output to the input. The outputs from both the MAIN and DLY ONLY LEVEL controls are mixed and applied to the EQ controls, which control the frequency response of the feedback chain.

The LOW EQ control adjusts the relative level of bass frequencies present in the feedback mix. When rotated counterclockwise, lows are cut; when rotated clockwise, they are boosted.

The HIGH EQ control has a corresponding effect on higher frequencies. When both controls are centered, the frequency response of the feedback chain is approximately flat.

The actual frequency corners and rolloff curves are available in the specifications section of this manual. Please note that one can set the FEEDBACK controls, deliberately or otherwise, to a point where loop gain exceeds 1 at various frequencies. It is possible, and even easy to obtain uncontrolled oscillation. For this reason, it is suggested that the operation of the FEEDBACK group be undertaken cautiously until the user is fully familiar with the possibilities for interaction of the various controls.

DELAY ONLY OUTPUT (MSEC) SWITCH GROUP

This group of switches controls the delay time of the DELAY ONLY output. Each switch is a push/ON push/OFF control which is active when the button is depressed. The numbers above each switch represent the number of milliseconds (1/1000 second) added to the time delay when that switch is active. For instance, if buttons 1, 2, and 6 are in and buttons 3,4, and 5 are out, the time delay at the DELAY ONLY OUTPUT would equal 6.25ms+12.5ms+200ms, or 218.75 milliseconds.

The switches may be activated in any combination. The maximum obtainable delay is equal to the sum of all the switches, 393.75 milliseconds, or about four tenths of a second. Setting the delay of the DELAY ONLY OUTPUT has no effect on, and is not affected by, any settings of the delay or mode controls associated with the MAIN OUTPUT.

PITCH CONTROL/READOUT GROUP

This block of controls is associated primarily with the manual/remote control of the output pitch ratio of the MAIN OUTPUT vs. the input signal. Only the general function of the controls will be described here as the precise function varies depending upon the operating mode set by the FUNCTION SELECT switch group.

The MANUAL pitch ratio control is an analog control which sets the Harmonizer to the desired pitch ratio. In the NORMal pitch change mode, the range of this control is approximately 2 octaves down (decreased pitch) to 1 octave up. This control also determines the rate of delay change in the FLANGE and RANDOM modes. See the table following this section for the range of this control in the various operating modes.

The PITCH RATIO indicator is a four digit LED display which, in all modes other than DELAY, shows the numerical pitch ratio between the INPUT and the OUTPUT. This ratio may be converted to musical intervals (thirds, fifths, etc.) by reference to the table in the appendix. As with the MANUAL control, its range varies depending upon the FUNCTION SELECTed. It also provides additional information in the FLANGE and RANDOM modes by giving a visual indication of the operation and rate of both functions.

Note that this readout is, in effect, a digital measuring instrument and may, absent malfunction, be relied upon to be absolutely correct plus or minus one least significant digit (.1%). The readout is also useful in calculating time speed-up and slow-down ratios when one desires to keep pitch constant and change the length of a tape recording. In such cases, proper pitch correction is obtained by setting the readout to the reciprocal of the tape speed ratio. Again, see the Appendix for information on performing these calculations.

The CONTROL MODE switch group permits selection of an EXTERNAL pitch control source. Depressing the MANUAL switch permits the MANUAL control to operate as just described. Depressing the CV+MAN switch permits summing a Control Voltage (input via the rear panel terminal block) with the MANUAL control. (Rear panel inputs are described in a later section).

Depressing the KEYBOARD switch permits phase locking the pitch control to an external control FREQUENCY. This control frequency may be generated from either a synthesizer VCO, or a special Eventide keyboard (Model HK940) designed to lock to the Harmonizer master oscillator and provide precise musical intervals upon demand. The control provided by the phase locking circuitry is far more precise than that provided by the Control Voltage circuit, and should be used whenever precise control of pitch ratio must be effected by an external source. The input signal requirements for frequency lock are covered in the section describing rear-panel connections.

REMOTE CONTROL OPERATION

The Harmonizer has provision for digital remote control via an optional circuit board and IEEE-488 connector on the rear panel. In normal (NON-REMOTE) operation, the LED adjacent to each of the CONTROL MODE switches mentioned above will illuminate RED when its corresponding switch is depressed. When the Harmonizer is operating under REMOTE CONTROL, whichever of the modes is active will be illuminated GREEN, both to signify the active MODE and to signify that the REMOTE CONTROL is determining the FUNCTION and CONTROL MODEs. The simultaneous illumination of all three GREEN lights signifies that the PITCH RATIO is being determined by the remote control unit and not by the front panel controls or rear panel inputs.

FUNCTION SELECT SWITCH GROUP

The FUNCTION SELECT push ON/push OFF switch and the four switches immediately to its right select the OPERATING MODE (as opposed to the control mode, described above) of the H949. This switch group determines, for instance, whether the unit is going to perform a pure delay or a pitch change function. The FUNCTION SELECT switch itself qualifies the operation of the actual control switches to its right. When the FUNCTION SELECT switch is OUT, the four controls select the functions labelled in GREEN immediately ABOVE each switch. When the switch is IN, the four controls select the functions labelled in RED immediately BELOW each switch. The RED/GREEN LED's above each of the four switches indicate which function is active by both selective illumination (only one of the four is ON), and by selective color (if the LED is RED, the function BELOW the switch is activated, if GREEN, the function ABOVE the switch is active).

The FUNCTIONS controlled by these four switches fall into two major groups: PITCH CHANGE EFFECTS (activated when the FUNCTION SELECT switch is IN, RED labels), and DELAY/REVERSAL effects (activated when the FUNCTION SELECT switch is OUT, GREEN labels. For clarity, the operation of the four switches will be described with relation to these two groups, rather than by discussing the functions of each physical switch.

PITCH CONTROL GROUP (RED)

When the FUNCTION SELECT is IN, the lower, RED labels of the function switches are effective. The leftmost switch, labelled "NORM", places the Harmonizer in the normal pitch change mode. Adjusting the MANUAL control over its full range gives pitch ratios from .25 (two octaves down) to 2.0 (one octave up. Note that the readout may exceed these ratios at the control extremes.

To assure adequate variation, the control is factory adjusted to provide extra range at each end. Although it is usually possible to dial ratios beyond the extremes given in the specifications, certain undesirable effects may become apparent: At the LOW end, decreasing the pitch ratio may increase the noise level, manifest symptoms of aliasing or heterodyning, and create other unpleasant digital sounding effects. At the HIGH end, increasing the reading beyond 2.00 will NOT increase the pitch ratio, but WILL create small amounts of undesirable phase noise.

The EXTENDed PC mode permits selection of the length of signal segment over which the pitch change algorithm operates. The NORM pitch change mode operates with a delay variation of approximately 25 milliseconds (see Theory of Operation). Depressing EXTEND allows extension of this segment to the full extent of the Harmonizer memory, or some fraction thereof, depending upon the setting of the MAIN OUTPUT (MSEC) DELAY S SWITCHES. (Normal operation of these switches is discussed under the next GROUP heading.) Special operations of these controls is also mentioned here, and under the REVERSE FUNCTION heading. When the rightmost three of these switches are physically OUT (normally inactive), the EXTENDed pitch memory segment covers the entire memory, 400 milliseconds. Depressing the 200 MILLISECOND (rightmost) switch cuts this memory segment by 200 milliseconds, to a total of 200 milliseconds. Depressing the 100 MILLISECOND switch (next to rightmost), the memory segment is DECREASED by 100 milliseconds, thus giving a total memory segment of 100 milliseconds. Depressing the 50 MILLISECOND switch decreases the memory segment to 50 milliseconds. Note that the operation of these switches may be regarded as reversed from their normal operation: Depressing the 200MS, 100MS and 50MS switches RESTRICTS the memory segment used by the pitch change mode by the amount indicated. If the 200MS switch is released (OUT), depressing the 100MS or 50MS switch will have no effect. If the 100MS switch is OUT, depressing the 50MS switch will have no effect.

UPC (MICRO PITCH CHANGE) modes, SHARP AND FLAT. These modes operate in a manner similar to the NORM PITCH CHANGE function, except that the range of pitch ratios is restricted to about 1:1.07 (SHARP) and 1:.93 (FLAT). Depressing the SHARP button allows adjustment of the pitch ratio from almost exactly 1:1 (unison) to approximately 1:1.07, corresponding to more than a musical "semitone". The pitch is adjusted using the MANUAL control, which now operates nonlinearly, so that as it is rotated closer to 1:1, the pitch change per degree of rotation decreases. This permits extremely fine and stable control of pitch ratios close to unity. It is easily possible to obtain an adjustment of 1.001 to 1, and have this remain stable over time and temperature within .1 per cent. This is better than an order of magnitude improvement over previously available units.

Depressing the FLAT button gives an adjustment range of approximately 1:1 to 1:.93, or more than one "semitone" down. Again, as the ratio approaches 1:1, the sensitivity of the ratio to the knob rotation decreases.

Note: For both SHARP and FLAT operation of MICRO PITCH CHANGE, the PITCH RATIO is closest to 1:1 when the MANUAL control is fully counter-clockwise. In SHARP, clockwise rotation INCREASES the pitch. In FLAT, clockwise rotation DECREASES the pitch.

DELAY/RANDOM/FLANGE/REVERSE FUNCTIONS (GREEN)

When the FUNCTION SELECT is OUT, the upper, GREEN labels of the function switches are effective. The first of these is the DELAY switch. When this switch is depressed, the MAIN OUTPUT acts like the DELAY ONLY output, and the IN/OUT pitch ratio remains at unity. The time delay is set by the MAIN OUTPUT (MSEC) switch group as described later.

Note: When in the DELAY mode, the MANUAL control affects the PITCH RATIO readout in the same manner as when the unit is in the NORM (PITCH CHANGE) mode. This is useful if one desires to pre-set the pitch ratio without changing the output signal: releasing the FUNCTION SELECT switch immediately acquires the selected pitch ratio. Remember: in the DELAY MODE, the pitch always remains at UNITY, regardless of other control settings or the PITCH RATIO readout.

RANDOM FUNCTION SELECT switch

Depressing this switch causes the MAIN OUTPUT to vary its delay between the maximum limits of 0 and 25 milliseconds at a constant rate of delay change. The actual delay limits, while restricted to the range given above, will typically be smaller on any given excursion. The range is determined in a "pseudo-random" manner by the Harmonizer's digital circuitry, and the effect created by using this mode closely simulates the random variations experienced when having individual performers "double" tracks, or having multiple musicians or singers performing simultaneously. Use of this operating mode is advantageous for "automatic double tracking" (ADT) because it gives a less "mechanical" sound than does fixed delay.

In the RANDOM MODE, the MANUAL pitch control varies the rate at which the delay varies from the upper to lower limit. Clockwise rotation increases the rate. Because the pitch varies slightly as the delay changes, the desirable effect of having the singers/performers very slightly out of tune is automatically achieved. The degree of pitch change may be reduced to a very small amount with the MANUAL control if so desired.

FLANGE FUNCTION Switch

This switch sets the Harmonizer into an automatic flanging mode. "Flanging" is the effect created when two signals of slightly differing delays are added together, while the delay of one signal is varying. (Delays on the order of 0 to 10 milliseconds are used. The lowest frequency affected is roughly the reciprocal of the time delay, so that a one millisecond delay causes cancellations at 1KHz and multiples thereof.) In the FLANGE mode, the MANUAL control varies the SWEEP rate, or the rate at which the delay of the variable delay signal is changing. Turning the MANUAL control clockwise increases the sweep rate.

Note: It is NOT necessary to mix the outputs of the MAIN and the DELAY ONLY outputs externally to achieve flanging. The DELAY ONLY output is unaffected by the FLANGE MODE, and the MAIN OUTPUT signal is flanged automatically.

RANDOM and FLANGE MODE NOTE:

To achieve normal FLANGING and RANDOM MODE operation, it is necessary for the ALGORITHM SELECT switch to be in the ALGORITHM 2 (physically OUT) position. If it is in the ALGORITHM 1 position, the output amplitude will vary with time and an extra delayed signal may be heard. The purpose of the ALGORITHM SELECT control is discussed later.

REVERSE FUNCTION switch

The final function switch controls the REVERSE mode of the Harmonizer. Activating

this mode causes the data entered into the memory to be read out backwards, so that short signal segments (up to the memory capacity of the Harmonizer) are presented in a time reversed order. The tape recorder analogy would be equivalent to cutting up a tape into 6 inch segments (at 15 inches per second) and then splicing the segments back into the same order after reversing the individual segments. Obviously this effect cannot reverse the time-order of entire programs as can playing a tape backwards, but the overall effect is the same except for signals which have very long attack or decay times.

The MANUAL pitch change control is active in the REVERSE mode and the pitch of the reversed signal may be altered within the same limits defined for the NORMal PITCH mode. There is no corresponding MICRO PITCH CHANGE mode for the REVERSE function.

Note that the REVERSE mode normally spans the entire Harmonizer memory of 400ms. If it is desired to reduce the length of signal segment acted upon by the reverse mode, one may restrict it by depressing the MAIN OUTPUT (MSEC) delay select switches as described in the EXTENDed PC mode. Depressing the 200MS button reduces the segment length to 200 milliseconds. Depressing the 100MS button reduces the segment length to 100 milliseconds, and depressing the 50MS button reduces the segment length to 50 milliseconds.

MAIN OUTPUT (MSEC) DELAY SET SWITCH GROUP

This group of 6 push/ON push/OFF buttons controls the delay of the MAIN OUTPUT. Depending upon the FUNCTION SELECTed, the switches may have other effects (see EXTENDed PITCH mode and REVERSE mode.) In the DELAY mode, all of the switches are active, and they operate in a manner precisely analogous to the DELAY ONLY OUTPUT (MSEC) switch group described earlier. In the DELAY mode, the MAIN OUTPUT DELAY is equal to the sum of the individual switches depressed.

In the NORM, MICRO PC, RANDOM, and FLANGE modes, only the last three switches are active. This is because the delay variation required by these functions is greater than the small increments of delay otherwise permitted. The MAIN OUTPUT, WITH THE EFFECT SELECTED, will be displaced by 50 to 350 milliseconds from its normal location in time, in accordance with the buttons depressed.

ALGORITHM SELECT 1/2

The ALGORITHM SELECT control determines the method the Harmonizer employs to handle the "glitches" which are a theoretical and practical consequence of the pitch change process. The word "algorithm" is defined as a precise, describable process which acts upon or modifies inputs in a specific manner. An algorithm may be simple or complex, although it must be defined under all circumstances. The characteristics of the two algorithms are described in greater detail in the Theory of Operation section.

Algorithm 2 is similar to that used in the Eventide Model H910 Harmonizer. It is characterized by "glitches" which occur at increasing frequency as the pitch ratio deviates from 1:1. Algorithm 1 does not produce glitches, but there is a varying degree of signal "coloration". For pitch ratios below .5 (one octave), algorithm 2 may produce hard "glitches" or clicks, and so algorithm 1 should be used at such extreme pitch errors.

Note: The proper selection of pitch change algorithm is a significant factor in the degree of success with which one can expect to modify the pitch of performed or recorded material. We recommend experimentation as the final arbiter of which is appropriate for any given program material and pitch ratio. The two algorithms converge in audible effect as the pitch ratios approach an octave in either direction, and both will perform identically at these extremes.

NOTE: See page 15 for use of the LV618 De-Glitch optional add-on board

FUNCTION	ALGORITHM	PITCH RATIO	CONTROL MODE
DELAY	-	.25-2.00	MAN,CV+M,KYBD
RANDOM	2 *	.99-1.01	MAN,CV+M
FLANGE	2 *	.99-1.01	MAN,CV+M
REVERSE	1 OR 2	.25-2.00	MAN,CV+M,KYBD
NORMAL PITCH CHANGE	1 OR 2	.25-2.00	MAN,CV+M,KYBD
EXTENDED PITCH CHANGE	1 OR 2	.25-2.00	MAN,CV+M,KYBD
MICRO PC SHARP	1 OR 2	1.0-1.1	MAN,CV+M
MICRO PC FLAT	1 OR 2	1.0-.90	MAN,CV+M

* Using algorithm #1 adds an extra delay to the output.

H949 Harmonizer - Chart showing which algorithm, pitch ratio, and control modes are operative for different functions.

REMOTE CONTROL

There will shortly be available a remote control option for the H949 which uses the IEEE/488 General Purpose Interface Bus to interface with a microcomputer. If information is not already printed in this manual, sending in the Warranty Card from the front of the manual will ensure that you are sent the information as soon as it becomes available.

VOLTAGE CONTROL OF PITCH RATIO

It is possible to remotely control the H949 Harmonizer pitch ratio by supplying a control voltage in the range from 0 to +10 VDC. An internal adjustment allows setting of the control voltage full scale between +5 VDC and +10 VDC, making it compatible with various synthesizers. The control voltage should be applied between terminal strip pins 10 and 11, with pin 11 being more positive. Care should be taken to ensure that the control voltage is as pure and free of ripple as possible, to avoid frequency modulation of the pitch shifted signal.

For your convenience, a source of clean +12 volts, current limited by a 10 k resistor, is available at pin 12 of the terminal strip. The equivalent input circuit at the CV IN pin is a 10 k resistor in series with an operational amplifier non-inverting input. Therefore, voltages within the range 0 to +12 will be feeding

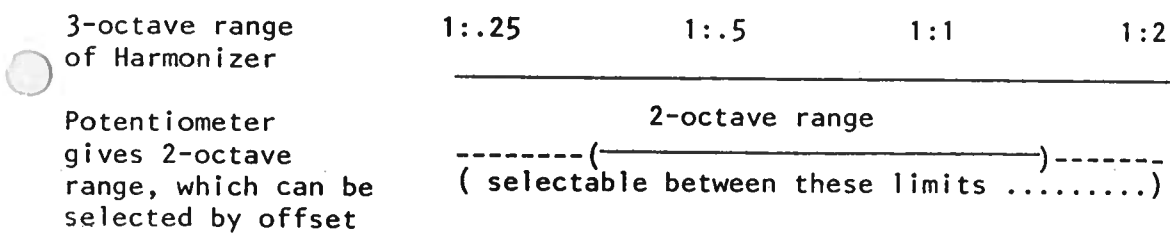
an essentially open circuit. Exceeding +12 volts will cause current to flow into the input, limited by the resistor. Greatly exceeding +12 volts may damage the input, and should be avoided.

Control voltage range adjustment

To adjust the external control voltage range, remove the Harmonizer top cover and swing the top board up on its hinges. The adjustment (labelled ECV LV) is a small trim resistor located about 3 cm in front of the keyboard Molex connector on the bottom circuit board.

RESISTIVE CONTROL OF PITCH RATIO

A remote control may be provided simply by connecting a 100 k potentiometer between terminal strip pins 12 and 10 and connecting the wiper to pin 11. The unit is factory set so that this connection will cover a two-octave range. The front panel manual pitch ratio control will provide an offset, enabling this two-octave range to be selected from the three-octave range of the Harmonizer.



Note: The maximum input voltage in this configuration is 10 volts.

FREQUENCY CONTROL OF PITCH RATIO

In addition to voltage control, the Harmonizer may be externally varied in pitch ratio by applying an input frequency from a signal generator, synthesizer, or other source. This mode is preferable to the Control Voltage mode for musical applications as the input frequency is precisely related to the pitch ratio, i.e., if the input frequency is increased by one interval, the pitch ratio likewise increases by one interval.

Signal requirements

The input frequency must be spectrally pure in that only the fundamental and its harmonics may be present. The unit will not accept signals with more than one fundamental frequency present, and should not be driven by any source from which a clean, constant signal level cannot be guaranteed. Function generator/synthesizer waveforms such as sine, square, and triangle waves are all acceptable.

The input voltage should be at least 5 volts peak to peak for a sine wave, and at least 3 volts for a square wave. All standard logic families meet these requirements.

Input frequency for unit pitch ratio is 2.5 kHz. Increasing or decreasing the input frequency by up to one octave up, or two octaves down, produces a corresponding change in the pitch ratio.

Tuning

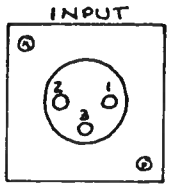
When using the Harmonizer with a customer-supplied keyboard, it may be necessary or desirable to re-tune the keyboard for a pitch ratio of 1.00 when middle C is depressed.

REAR PANEL CONNECTIONS

AC POWER CONNECTOR

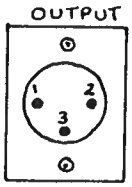
This connector accepts an internationally-approved IEC connector. The line cord furnished with the unit is for United States standard 3-wire outlets. The line voltage is specified on the serial number plate. It may be changed from 120 VAC to 240 VAC (or vice versa) by sliding the clear panel over the AC connector, removing the small printed circuit board, turning it round, reinserting it, and changing the fuse to the correct value (½ amp for 120 VAC, 3/8 amp for 240 VAC, slo blo type).

INPUT CONNECTOR (3-pin XLR female)



This is the audio input connector for the H949 Harmonizer. Refer to the Specifications for levels and impedances.

OUTPUT CONNECTORS (3-pin XLR male)



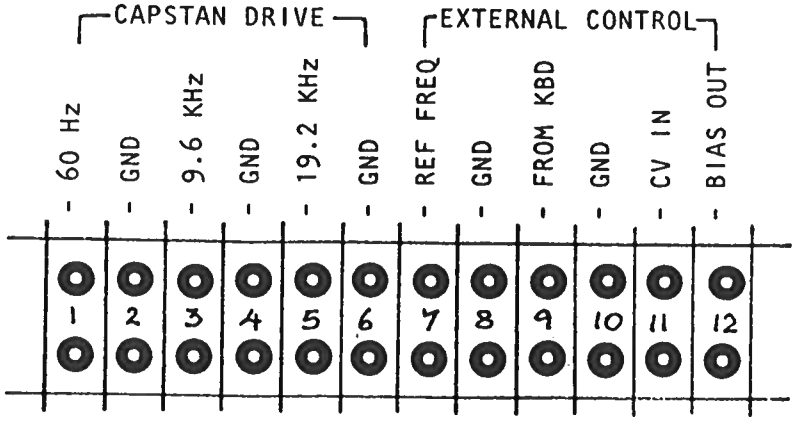
Each output has an output connector for audio. Refer to the Specifications for levels and impedances.

Pin 1 is shield/chassis ground
Pin 2 is output - phase
pin 3 is output + phase

KEYBOARD CONNECTOR, REMOTE CONTROL (IEEE/488) CONNECTOR

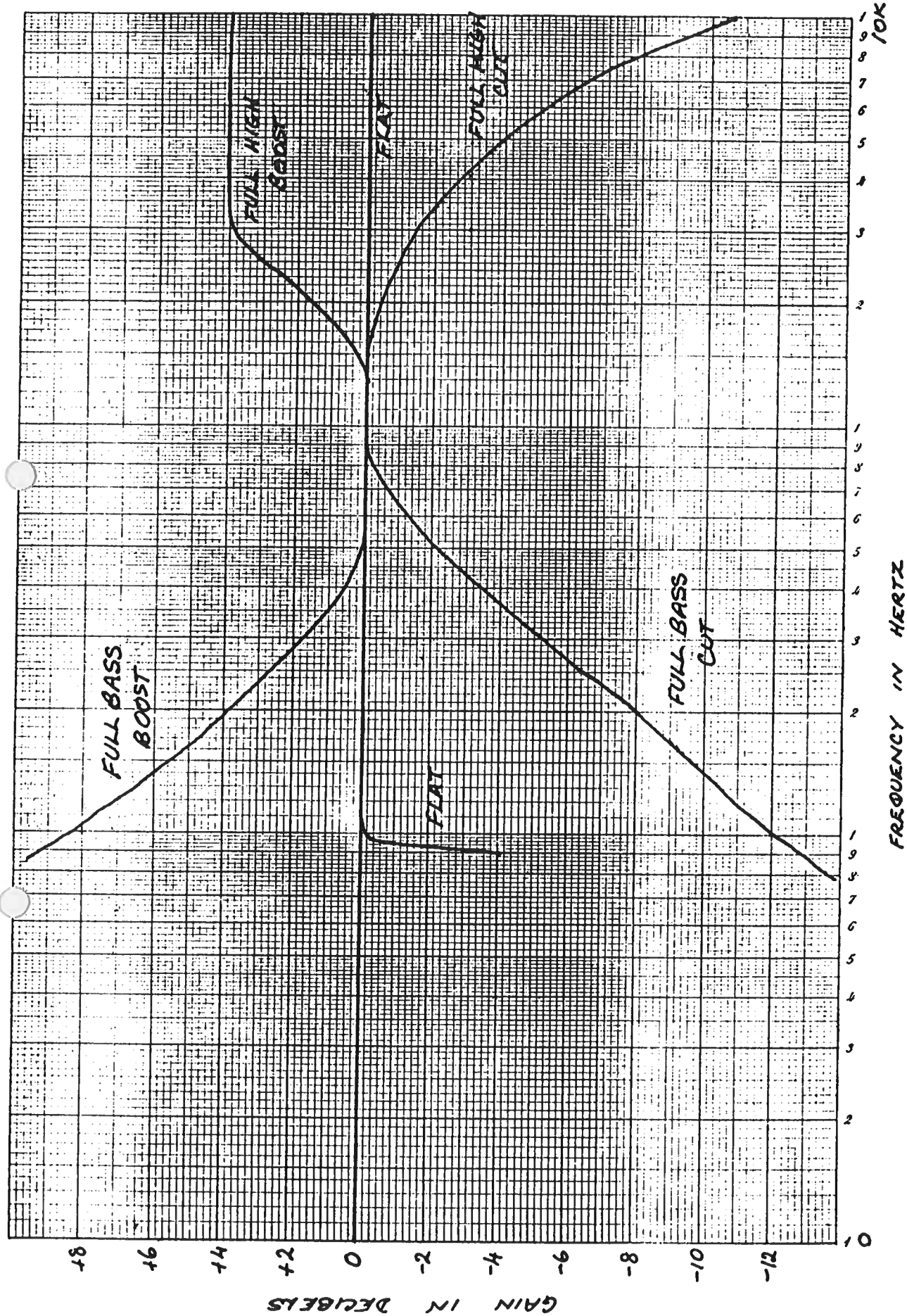
Refer to Keyboard and Remote Control sections of manual for details.

CAPSTAN DRIVE AND EXTERNAL CONTROL TERMINAL STRIP



GROUNDING

As with any piece of audio equipment, good grounding practices should be followed when connecting the unit. The grounds should be connected insofar as possible as shown above. This will help prevent ground loops and subtle troubles that can occur when equipment to be interconnected is at differing ground potentials. A sure sign of grounding problems is if an unexplained hum or buzz is present even when the LINE switch of the Harmonizer is in the OUT position. The LINE switch bypasses the unit with a DC path, and is independent of whether power is applied. While the Harmonizer is susceptible to certain faults and component breakdown, it is unlikely that generating hum or buzz is among them. If the unit seems to be contributing such a signal, and there is no evidence that the power supply is faulty, check your grounding scheme first of all. Incidentally, this applies to almost all accessory equipment.



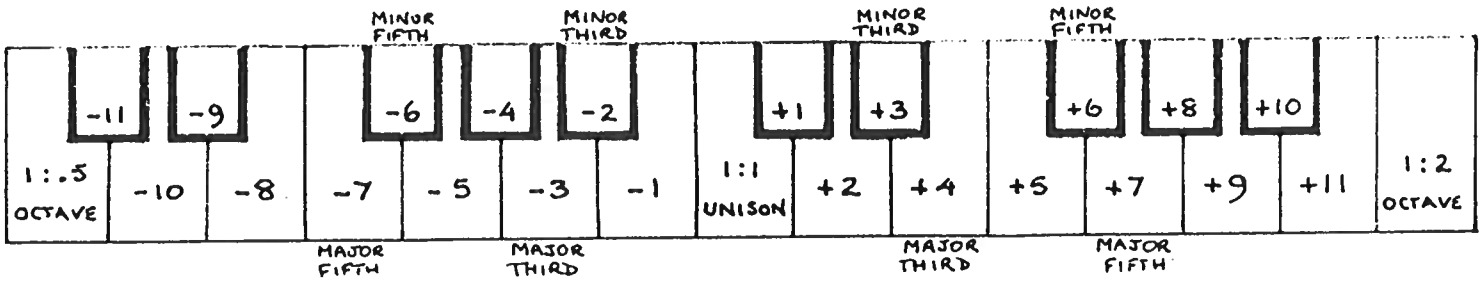
FEEDBACK EQUALIZATION FREQUENCY RESPONSE

PITCH RATIO READOUTS FOR VARIOUS MUSICAL RELATIONSHIPS

-3/4	-1/2	-1/4	NOTE	RELATIONSHIP	NOTE	+1/4	+1/2	+3/4
.958	.972	.986	1.000	UNISON	1.000	1.015	1.029	1.044
.904	.917	.930	.944	-1 +1	1.060	1.075	1.091	1.106
.853	.866	.878	.891	-2 +2	1.123	1.139	1.155	1.172
.805	.817	.829	.841	-3 +3	1.189	1.207	1.224	1.242
.760	.771	.782	.794	-4 +4	1.260	1.278	1.297	1.316
.717	.728	.738	.749	-5 +5	1.335	1.354	1.374	1.394
.677	.687	.697	.707	-6 +6	1.414	1.435	1.456	1.477
.639	.648	.658	.667	-7 +7	1.498	1.520	1.542	1.565
.603	.612	.620	.630	-8 +8	1.587	1.611	1.634	1.658
.569	.578	.586	.595	-9 +9	1.681	1.706	1.731	1.756
.537	.545	.553	.561	-10 +10	1.781	1.808	1.834	1.861
.507	.515	.522	.530	-11 +11	1.888	1.915	1.943	1.971
.479	.486	.493	.500	OCTAVE	2.000			
.452	.459	.465	.472	-13				
.427	.433	.439	.446	-14				
.403	.407	.414	.420	-15				
.380	.381	.391	.397	-16				
.359	.364	.369	.375	-17				
.339	.344	.349	.354	-18				
.320	.324	.329	.334	-19				
.302	.306	.310	.315	-20				
.285	.289	.293	.297	-21				
.269	.273	.277	.281	-22				
.254	.257	.261	.265	-23				
			.250	TWO OCTAVES				

Note: The lowest octave is only available with the H949.

For use with the H910 Harmonizer, round off the figure to two decimal places.



PITCH CHANGE

The Eventide Harmonizers model H910 and H949, and 1745M Delay Line with Pitch Change Module may be used to generate musical harmonies by reference to the above table. Because a digital compression or stretching process is used, all harmonic relationships are preserved, unlike the disharmony produced by heterodyne-type 'frequency shifters'.

For example, suppose two frequencies, originally in a musical relationship, are shifted up by 100 Hz. Although the absolute difference between the signals remains constant, the musical interval between them decreases. However, if the two frequencies are *multiplied* by any constant, as in the Harmonizers and Pitch Change Module, the interval remains constant, even though the absolute difference will change.

TEMPO REGULATION

The internal oscillator of the 1745M and the H949 Harmonizer provides an output frequency which may be used to control the speed of a tape recorder. The H910 Harmonizer does not have this facility.

The H949 back panel terminal strip provides output frequencies of 19.2 kHz, 9.6 kHz, and 60 Hz. These are three of the major standards for servo-controlled tape machines.

When the tape machine is being controlled by the H949 capstan drive output frequency, a pitch ratio of unity (1.000) will result in the tape running at normal speed. A ratio above unity will result in a slower tape speed, and a pitch ratio below unity in a faster tape speed.

One of the primary uses of this feature is in time compression. Suppose, for example, that you have a commercial which is intended for a 60-second time slot, but the commercial actually runs for 62 seconds. The required pitch ratio may be ascertained as follows:

60 / 62 = 0.968 (rounded to four digits)

The tape speed will be increased slightly.

If, as is usually the case, the required pitch ratio falls into the range from 1.08 to 0.92, it is recommended that you use the MICRO PITCH CHANGE mode, which will avoid any tape speed problems (see note below), and also help to stabilize the pitch setting.

Because of the Harmonizer 'glitch', it may be advisable to record the passage more than once, and select the best portions from each recording.

NOTES:

See Technical Section page T3 for instructions on aligning the CAP CAL trimpot.

Depending upon the input drive requirements of the tape machine, it may be necessary to buffer the H949's capstan drive output with an external amplifier.

VERY IMPORTANT. While pitch ratios above unity will not cause the tape machine any problems, it is essential to remember that, if normal tape speed is 30 ips, a pitch ratio of .5 (one octave down) will result in a tape speed of 60 ips, and a pitch ratio of .25, two octaves down, will result in a tape speed of 120 ips and almost certain chaos!

On the next page you will read some information about two additions for the H949 Harmonizer, both of which are very useful for time compression applications. YOU WILL RECEIVE FURTHER INFORMATION ON THIS AND OTHER NEW PRODUCTS IF YOU RETURN YOUR WARRANTY CARD (which is at the beginning of the manual).

DE-GLITCH AND REMOTE OPTIONS FOR H949 HARMONIZER

LU618 DE-GLITCH BOARD FOR H949 HARMONIZER

The LU618 is a signal processor/analyzer board which eliminates almost completely the "glitching" characteristic common to all pitch change devices which operate by eliminating or adding signal segments. This computerised addition to the H949 determines the optimum splicing point, thus reducing the potential "glitch" to inaudibility in most cases.

As the LU618 board uses a degree of "intelligence" to decide the optimum splicing point, it works best on single-instrument program material. If the program material is too "busy", the improvement may not be as great.

The LU618 board mounts just underneath the HD921 digital board inside the H949 Harmonizer. If this board has been installed at the factory, the serial number plate of the unit will read "option: ALG.3".

The "de-glitch" mode is in operation when ALGORITHM 2 is selected.

Algorithm 1, which gives a somewhat softer splice, resulting in a tremolo effect, may be preferred for certain special effects. We suggest that you experiment to see which suits your program material best.

NOTE: The de-glitch splicing method is only operative in NORMAL and MICRO PITCH CHANGE. It is not operative in REVERSE or EXTEND modes.

As the de-glitch board makes the H949 Harmonizer almost entirely glitch-free, it will probably temd to be the preferred setting for most work.

The LU618 de-glitch board may be added in the field to any H949 Harmonizer with a serial number after A949-1606. It may be added to earlier units at the factory. Call Eventide or your local dealer for price and delivery.

COMPUTER REMOTE CONTROL BOARD FOR H949 HARMONIZER

This board enables almost all the functions of the H949 Harmonizer (including pitch change) to be controlled by an external computer. The board uses the IEEE-488 standard, which permits multiple units to be controlled individually on a single bus, thus reducing the cost and complexity of interconnection.

The board is completely compatible with the IEEE-488 standard, and can be controlled by low-cost home computers (such as the Commodore PET or Hewlett-Packard model 85), as well as by several automated consoles and industrial computers.

Harmonizer is Eventide's trade name for a special effects device including pitch change.

THINGS NOT TO WORRY ABOUT

This is a list of things which may seem strange but are really normal in the H949 Harmonizer.

* The rear panel regulator is exposed, yet mounted on a mica insulator. The insulator is to prevent hum in the output. THERE IS NO EXPOSED HIGH VOLTAGE on the regulator.

* When switching from PITCH to DELAY, it is not unusual to observe a small level shift (a fraction of a dB). This is of no consequence, either in operation or for maintenance. If the level shift exceeds 1 dB, it should be investigated. (See Alignment Section.)

* The PITCH RATIO READOUT will occasionally flash (blank) for a few milliseconds between readings. This is a characteristic of the counter chip, and should be ignored. Frequent blanking, several times in a ten-second period, may be indicative of a readout problem. This will RARELY IF EVER create an AUDIO problem.

* The LAST DIGIT of the readout will usually vary +/- one digit. This is a theoretical consequence of digital counting and does not indicate a corresponding variation in pitch ratio. In the UPC (micro pitch change) mode, the last digit may also DRIFT over time and temperature, and in the NORMAL PC mode, the second-from-last digit may drift over time and temperature. A variation of .1% in UPC and 1% in NORMAL PC is within tolerance. Excessive drift may be caused by unusually high line voltage, or lack of ventilation, or by defective components.

* Power line outages, or turning the Harmonizer OFF and then ON rapidly may initiate a mode of operation in which the UPC directions are reversed (flat becomes sharp) and FLANGE and RANDOM do not work. This occurs because the power ON reset circuitry requires time to discharge on power OFF. This problem may be remedied by turning the unit OFF for about five seconds before turning it ON again.

* The SIGNAL PRESENT LED does not go on at a precisely defined level, but rather is intended to show that a signal is present. It should always be OFF when the input level control is at zero, or there is no input signal (providing that the FEEDBACK controls are off). It should always be ON when the input signal exceeds -30 dB with respect to clipping. It may come ON at any level between these broad limits.

* It is possible, but very unlikely, for the PITCH CHANGE circuitry to go 'out of sync', introducing distortion at the main output. If this happens, the circuitry can be reset, either by changing the main output function, or by turning power OFF, waiting five seconds (see above) and then ON again.

* When operating in the External Control modes, the pitch ratio readout may indicate ratios above 2.00. However, the actual ratio will be limited to 2.00, regardless of the reading. Note that the pitch ratio readout continues to operate even in the DELAY mode. This is of advantage because it permits one to set a precise ratio and then switch from DELAY to that ratio by going into the PITCH CHANGE mode.

HK940 - KEYBOARD FOR EVENTIDE HARMONIZER MODEL H910 AND MODEL H949

The two octave phase locked keyboard is available in two versions - option 05, mono, for controlling one Harmonizer, and option 06, polyphonic, for controlling one, two, or three Harmonizers. The mono keyboard cannot be 'upgraded' to polyphonic.

The keyboard controls the pitch ratio of the Harmonizer(s) in discrete musical steps. Middle C on the keyboard is 1.00 on the readout - a one-to-one pitch ratio (unison). Playing the E above middle C will give a harmony of a major third, playing E flat will give a minor third, and so on.

When the polyphonic keyboard is being used to control three Harmonizers, the first key pressed controls Harmonizer #1, the second key pressed (while holding the first) controls Harmonizer #2, and the third key pressed (while still holding the first and second) controls Harmonizer #3. Releasing any of these keys and pressing another will change the pitch of that Harmonizer only.

The keyboard GLIDE pot affects Harmonizer #1 only. The pitch change action ranges from instantaneous to a gentle slide. There is a LOCK switch for each Harmonizer, which holds the Harmonizer at the last note pressed. In non-LOCK mode, the Harmonizer(s) will return to middle C in the absence of any key depression.

No music is generated in the keyboard. Your music, passing through the Harmonizer, is pitch changed on instruction from the keyboard. The keyboard/Harmonizer combination can be used as a musical instrument if the Harmonizer input is supplied with middle C (approximately 260 cycles) of the waveform or timbre you require.

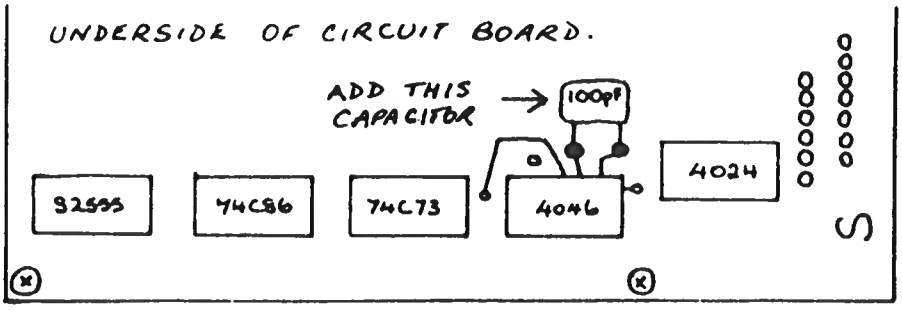
The keyboard is basically an electronic clock, with some sequencing and timing circuitry. The keyboard is slaved to the Harmonizer clock (Harmonizer #1 for the poly keyboard) for perfect unison at middle C. Keyboard keys select appropriate timing pulses, which command the desired pitch change in the Harmonizer.

Use of the HK940 Keyboard with Model H949 Harmonizer

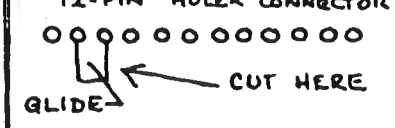
(REVERSE THIS MODIFICATION TO USE A H949 KEYBOARD WITH THE H910)

The H949 Harmonizer can lower the pitch of an input signal by two octaves. The keyboard does not control this lower octave.

For use with the H949 Harmonizer, the keyboard requires the following modification. With keys towards you, loosen the left wooden side enough to allow removal of the top cover. Underneath is the underside of the circuit board. Add a 100 pF DM15 capacitor, as shown. Replace the top cover, and tighten the left side.



On the HA931 analog board, make the cut as shown:



NOTE: If the keyboard was supplied for use with a 949 Harmonizer, the modification has been done already.

INTERCONNECTION OF HK940 KEYBOARD WITH EVENTIDE HARMONIZER MODELS H910 & H949

1. Harmonizer with mono keyboard, and Harmonizer #1 with poly keyboard, should be equipped with a keyboard socket on the Harmonizer rear panel.

   a) If no socket is supplied, ask your dealer to provide one.
   NOTE: every H949 is fitted with a socket already.

   b) If the socket is supplied but not installed, proceed as follows:

      i. screw socket into rear panel of Harmonizer (remove blanking plate).

      ii. plug connector M3 together (observe polarity).

      iii. remove shorting connector from M4. KEEP IT SAFELY! It will be needed if you ever require to use the Harmonizer with a synthesizer keyboard or similar.

      iv. plug connector M4 together (observe polarity).

   c) Connect keyboard cable to socket on Harmonizer rear panel.

   d) H910: Press KBD switch on Harmonizer front panel.
   H949: Select KEYBOARD control mode on Harmonizer front panel.

2. Harmonizer #2 or #3 with poly keyboard

   a) For H910 Harmonizers only:
   If Harmonizer has a keyboard socket, this must be disconnected from M3 and M4, and shorting plug replaced on M4 (observe polarity).

      i. If you have lost the shorting plug, the two pins to be shorted together are (counting the pin nearest the front panel as #1) pin #2 and pin #3.

   b) A cable which is phone plug to two lug connectors is supplied. Connect phone plug to jack H2 or H3 on keyboard rear panel.

      H910: Connect red lug to terminal 3 of Harmonizer (see page 3 of manual: terminal 3 is Remote Control Frequency IN). Connect black lug to terminal 4 of Harmonizer (Remote Control GROUND).

      H949: Connect red lug to terminal 9 of Harmonizer (External Control FROM KYBD).
      Connect black lug to terminal 10 of Harmonizer (External Control GROUND).

   c) H910: Press KBD switch on Harmonizer front panel.
   H949: Select KEYBOARD control mode on Harmonizer front panel.

Eventide harmonizer model H949

TECHNICAL SECTION

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ALIGNMENT INSTRUCTIONS

The trimpots referred to in the following instructions may be located on the 949's circuit boards by consulting the topological drawing in the section on each board.

AUDIO ALIGNMENT

NOTE: For the following adjustments both FEEDBACK level controls should be OFF, DELAY should be set to zero for each output, and ALGORITHM 2 should be selected unless otherwise indicated.

COMPRESSOR DISTORTION AND LEVEL ADJUSTMENT

1) Apply a +6dBm 1kHz low-distortion sine wave to the 949.
2) Turn the INPUT LEVEL knob until the sine wave appears clipped at the COMPRESSOR input.
3) Reduce the input signal level by 3dB.
4) Adjust the COMPRESSOR GAIN trimpot (G) so that the red LIMIT LED just begins to light.
5) Attach the distortion meter to the COMPRESSOR output.
6) Adjust the HIGH FREQUENCY DISTORTION trimpot (H) for minimum distortion.
7) Reduce the input sine-wave frequency to 100Hz.
8) Adjust the LOW FREQUENCY DISTORTION trimpot (L) for minimum distortion.
9) Repeat steps 4-8 as necessary.

OFFSET ADJUST

1) Apply a 1kHz, +6dBm sine-wave to the 949.
2) Adjust the INPUT LEVEL pot so that the LIMIT LED begins to light.
3) Reduce the input signal level by 45dB.
4) Adjust the OFFSET trimpot so that the yellow PRESENT LED just turns off or is flickering.

NOTE: If a significant adjustment of the OFFSET trimpot (greater than 10 degree rotation) is necessary, the COMPRESSOR DISTORTION AND LEVEL ADJUSTMENT should be repeated.

MAIN OUTPUT DISTORTION AND LEVEL ADJUSTMENT

1) Select MAIN OUTPUT RANDOM FUNCTION, KEYBOARD CONTROL MODE (PITCH RATIO should read 1.000).
2) With a 1kHz signal applied to the input, set the INPUT LEVEL pot so that the top GREEN level LED just begins to turn on.
3) Adjust the MAIN OUTPUT EXPANDER GAIN trimpot (G) for a peak-to-peak swing of 20 volts.
4) Reduce the input signal by 3dB and adjust the HIGH FREQUENCY trimpot (H) for minimum distortion.
5) Reduce the input frequency to 100Hz.
6) Adjust the LOW FREQUENCY trimpot (L) for minimum distortion.
7) Increase the input signal by 3dB and re-adjust the GAIN trimpot for a 20 volt output swing.
8) Select DELAY FUNCTION
9) Adjust the DELAY LEVL trimpot on the top board, HD921, for a 20 volt output swing.

DELAY OUTPUT DISTORTION AND LEVEL ADJUSTMENT

Follow steps 1-7 described above for MAIN OUTPUT.

FEEDBACK LEVEL

1) Select MAIN OUTPUT DELAY FUNCTION.
2) Apply a 1kHz input signal with sufficient level to light the LIMIT LED.
3) Set MAIN DELAY equal to 200 msec.
4) Set both FEEDBACK EQ pots to FULL CUT.
5) Turn MAIN FEEDBACK LEVEL pot full clockwise.
6) Turn INPUT LEVEL pot off (counter clockwise) and observe output signal.
7) Adjust FEEDBACK LEVL trimpot so that output decays gradually.

TIMING AND CONTROL ALIGNMENT

The following alignment instructions should be followed carefully and in the indicated sequence to assure proper performance.

MASTER OSCILLATOR TUNING

1) Connect frequency counter (or 'scope) to PIN 7 of IC47.
2) Swing board up and adjust COIL (variable inductor) using a plastic hex alignment tool for a frequency of 40.96kHz
CAUTION-Take care not to crack the brittle tuning slug.

MANUAL CONTROL

1) Select NORMAL pitch change mode and MANUAL CONTROL MODE.
2) Rotate MANUAL pot fully counter-clockwise and adjust trimpot MINF, located on front panel board HP941 for a PITCH RATIO of approximately .240.
3) Rotate MANUAL pot fully clockwise and adjust trimpot MAXF, located on lower board HA931, for a PITCH RATIO of approximately 2.10.
4) Repeat steps 2 & 3 as necessary.

EXTERNAL CONTROL VOLTAGE

1) Select NORMAL pitch change mode and MANUAL CONTROL MODE.
2) Adjust MANUAL pot for PITCH RATIO of 1.00.
3) Select CV+MAN CONTROL MODE.
3) Apply minimum desired control voltage to the rear panel terminal strip input CV IN.
4) Adjust trimpot ECV OFFSET for a PITCH RATIO of .500
5) Apply maximum desired control voltage to CV IN.
6) Adjust trimpot ECV LEV for a PITCH RATIO of 2.00
7) Repeat steps 3, 4, 5 & 6.

The 949 is factory adjusted for a +12 volt to ground ECV range so that the pitch can be controlled by an external potentiometer connected to the BIAS OUT rear panel terminal.

SINGLE SIDE BAND GENERATOR

NOTE: This adjustment should not be performed without using a SPECTRUM ANALYZER capable of resolving an 82kHz signal with 300Hz sidebands. Fortunately this adjustment is not very critical; re-adjustment should be necesary only if one of the modulator IC's (IC's 38 & 39) is replaced.

1) Set SPECTRUM ANALYZER for a center frequency of 82kHz and resolution of 300Hz.
2) Attach SPECTRUM ANALYZER to PIN 1 of IC41.
3) Select uPC# function and MANUAL CONTROL MODE with the MANUAL pot set at twelve o'clock.

4) Null 82kHz signal by alternately adjusting trimpots SSB1 and SSB2.
5) Select uPCb.
6) Repeat step 4.

TAPE CAPSTAN DRIVE

1) Disconnect keyboard (if necessary).
2) Select KEYBOARD CONTROL MODE.
3) Connect frequency counter (or 'scope) to the 19.2kHz CAPSTAN DRIVE terminal strip output.
4) Adjust trimpot CAP CAL for 19.2kHz

SERVICE SECTION

INTRODUCTION TO SERVICE SECTION

The circuitry of the H949 is contained on three printed circuit boards, with the exception of the unit's power transformers, a bridge rectifier, and three of the voltage regulators. These conponents are mounted on the right side and rear panels of the chassis. The part numbers of the three circuit boards are:

1) HA 931 Rev _ -Mounted horizontally on the bottom of the chassis. HA 931 contains power supply, audio processing, pitch change timing and function control circuitry. It is attached to the chassis at the rear panel terminal strip and to the bottom cover by 8 size 4-40 screws.

2) HD 921 Rev _ -Supported by five stand-offs above HA931 and attached to the rear panel by two hinged stand-offs. When the five size 6-32 screws are removed HD 921 can be swung up on its hinges allowing "power-on" access to the lower and front panel boards.

3) HP 941 Rev _ -Mounted vertically behind and attached to the front panel by six stand-offs, it supports all front panel switches with the exception of the line and power switches. It also supports the PITCH RATIO READOUT and all indicator LED's. Mounted on HP941 is the following: AUDIO FEEDBACK, READOUT timing and DELAY SET circuitry.

POWER SUPPLY

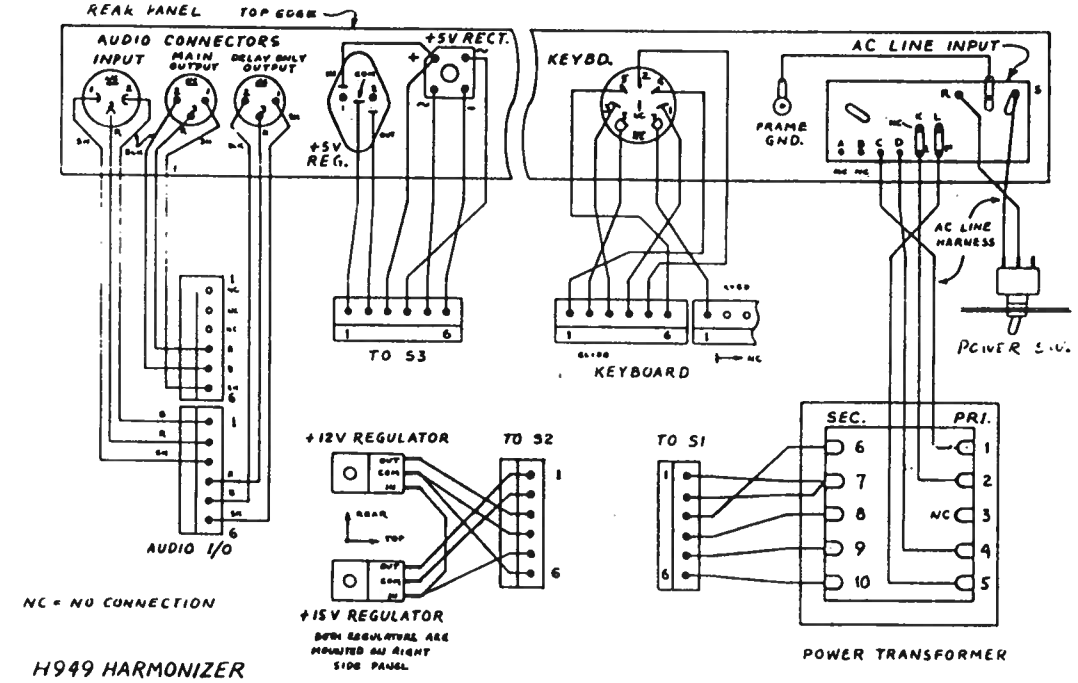
The 949's power supply provides regulated +15, -15, +12 and +5 DC volts to the circuitry contained on the three p.c. boards. The power supply circuitry is mounted on lower p.c. board HA 931 and the right and rear chassis sides.

The AC input receptacle is mounted on the rear panel and accepts a standard IEC line cord. The receptacle also contains the unit's 1/2 amp "slow-blow" fuse (3/8 amp for 230 volt operation) and a small plug-in circuit card which determines the operating line voltage. This permits conversion to and from 230 volts without removing the unit's covers.

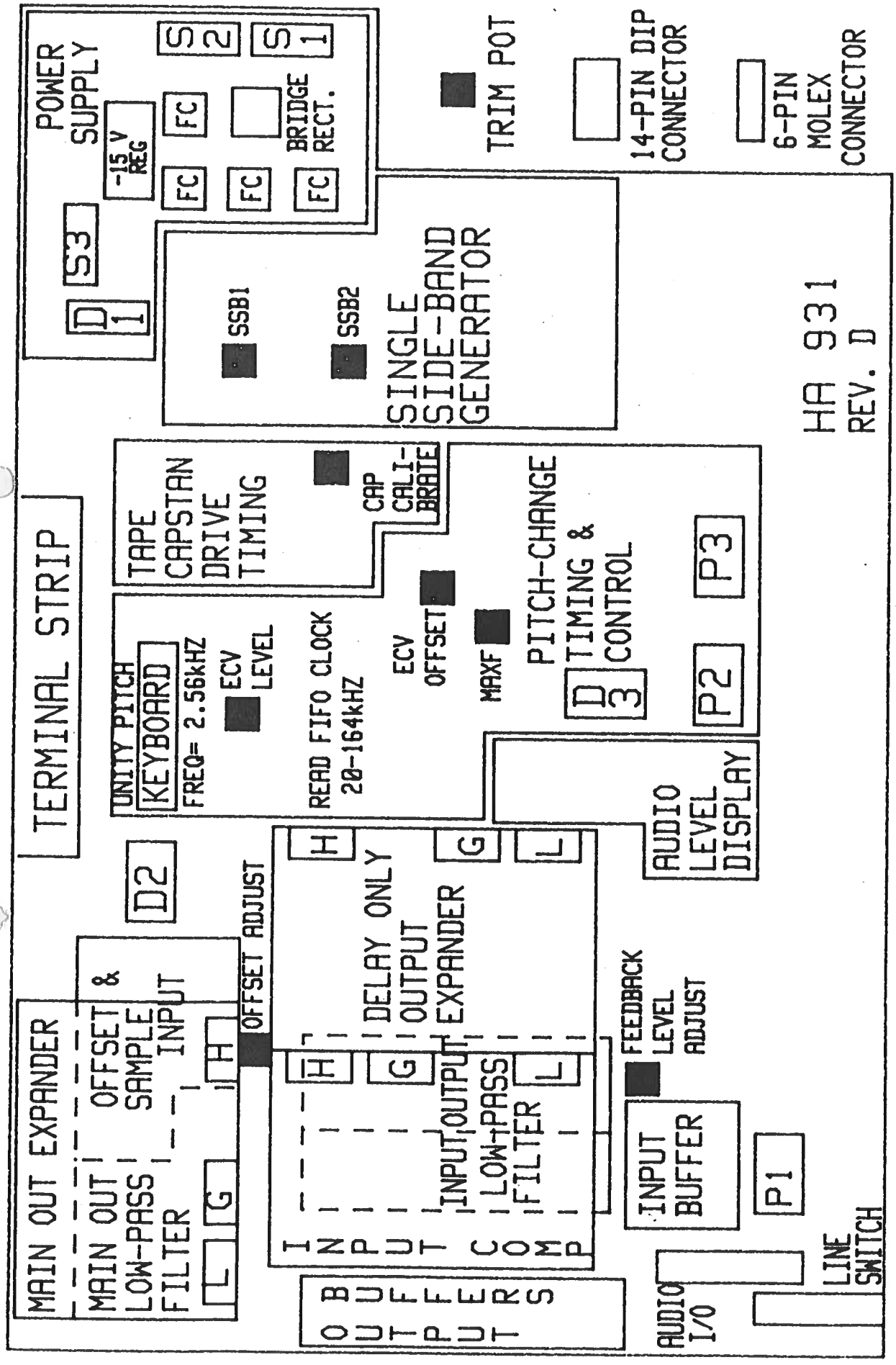
Line voltage is connected to the POWER TRANSFORMER's primary windings (mounted on the right side of the chassis) via the front panel POWER switch. The power transformer has two secondary windings; one low voltage-high current for the +5 volt supply and the other high voltage-low current for +15, +12, and -15 volts. The secondary windings are connected to HA 931 via 6 conductor Molex connector S1.

The +5 volt winding is routed directly to Molex connector S3 which is connected to a 5-amp bridge rectifier and 3-amp LM323 voltage regulator which are mounted on the rear panel heat sink. The rectifier output (approx. +8.5 volts unregulated) and the regulator output (regulated +5 volts) return to HA 931 via S3. The rectifier output is connected to the electrolytic filter capacitor mounted on HA 931.

The other transformer secondary is connected to a bridge rectifier mounted on HA 931. Both a positive and negative rectified voltage are output from the bridge and filtered by a pair of electrolytic capacitors. The negative voltage is input to a 1/2-amp, -15 volt regulator, LM7915, mounted on HA 931. The positive rectified voltage is routed, via Molex connector S2, to two 1/2-amp positive voltage regulators, LM78M12 (+12 volts) and LM7815 (+15 volts), mounted on the right side of the chassis. The regulator outputs return via S2.



H949 HARMONIZER
REAR AND RIGHT SIDE PANEL
WIRING HARNESSES


POWER SUPPLY
-15 V REG
FC
FC
FC
FC
BRIDGE RECT.
S2
S1
S3
D 1
TRIM POT
14-PIN DIP CONNECTOR
6-PIN MOLEX CONNECTOR
SSB1
SSB2
SINGLE SIDE-BAND GENERATOR
HA 931 REV. D
TAPE CAPSTAN DRIVE TIMING
CAP
CALI-BRATE
UNITY PITCH KEYBOARD
FREQ= 2.56kHZ
ECV LEVEL
READ FIFO CLOCK 20-164kHZ
ECV OFFSET
MAXF
PITCH-CHANGE
D 3 TIMING & CONTROL
P3
P2
AUDIO LEVEL DISPLAY
TERMINAL STRIP
D2
OFFSET ADJUST
H
G
L
DELAY ONLY OUTPUT EXPANDER
MAIN OUT EXPANDER
MAIN OUT LOW-PASS FILTER
OFFSET & SAMPLE INPUT
L
G
H
INPUT
OUTPUT
LOW-PASS FILTER
FEEDBACK LEVEL ADJUST
INPUT BUFFER
P1
OUTPUT TRANSFORMER
AUDIO I/O
LINE SWITCH

AUDIO PROCESSING

The three rear panel XLR connectors, AUDIO INPUT, MAIN OUT, and DELAY ONLY OUT, terminate at a twelve-pin Molex connector AUDIO I/O which is connected to the six-pole, double-throw LINE SWITCH. When the switch is in the OUT position, the audio signal by-passes the unit (the input XLR is connected directly to both output XLR's) and isolates the audio signal from the circuitry of the 949. This is an important diagnostic feature allowing the user to test the external audio cables independent of the 949's circuitry. When the LINE SWITCH is IN the audio input is applied to the 949 and the output XLR's are connected to the unit's output drivers.

INPUT PROCESSING

The differential input signal is buffered and converted to a single-ended signal by three of the op-amps of quad op-amp IC1. The signal is routed, via fourteen-pin connector P1, to the front panel and the INPUT LEVEL potentiometer. It returns via P1, and is summed with the FEEDBACK signal by the remaining op-amp of IC1. The signal is then low-pass filtered by a seven-pole, four-zero "Cauer-Chebychev" filter (one-half of quad op-amp IC's 2 and 3 and one-half of dual op-amp IC4) and compressed by a plug-in DBX 303 card (compression ratio 2/1). For proper adjustment of the DBX "distortion null" and "gain" trimpots, refer to the ALIGNMENT section of the manual. A DC-coupled inverting amplifier (one-half of IC6) superimposes a +5 volt DC bias on the signal, which is then sampled by analog switch IC8 and stored on the .001uF HOLD capacitor. Due to the unipolar nature of the analog switch, the audio signal is limited to a maximum voltage swing of 0 to + 10 volts. The sampled voltage stored on the HOLD capacitor is linearly discharged by a "constant current sink", (comprising a 2N3391 transistor, a 1N753 Zener diode, a 1N914 silicon diode, and associated passive components), while being compared to 0 volts by an analog comparator IC9. The comparator output signal, CMP, is a pulse whose width is proportional to the sampled voltage. The pulse-width modulated signal is then routed to the upper p.c. board HD921 where it is converted to a digital code as described later. Trimpot OFFSET ADJUST varies the HOLD capacitor discharge rate by varying the constant current sink. For proper adjustment of this trimpot refer to the ALIGNMENT section of this manual.

OUTPUT PROCESSING

The two output signals from connector D2, MDAC and DDAC, are applied to their respective low-pass filters, expanders, and output buffers. The main output signal MDAC is filtered by IC6 and one-half of IC5, expanded by a DBX 303 card (2/1 expansion ratio) and converted to a differential audio signal by one-half of IC7. Each phase of the output signal is driven by a complementary pair of transistors which provides greater output current capability into low impedance loads.

The DDAC output signal is processed identically to MDAC; filtered by one-half of IC's 2, 3 and 4, expanded by a third DBX card and converted to a differential audio signal (second-half of IC7).

PITCH CHANGE TIMING AND CONTROL CIRCUITRY

The pitch change functions of the 949 are accomplished by storing (or "writing") digitized audio at a fixed rate and retrieving it ("reading") at a variable rate. To increase pitch, one reads the data at a faster rate than that at which it was written; to decrease pitch, one reads the data at a slower rate than written.(The similarity to tape machine pitch change should be apparent). Of course matters are not quite this simple; there is a rub.

THE RUB: Let's suppose we are increasing the pitch of an audio signal as described above. We must remove data samples faster than we are storing them, eventually emptying our data store. At this point we are forced to stop outputting data and, not surprisingly, this does not sound very good. A moment's reflection will reveal that a similar problem arises when attempting to decrease pitch in this manner. This underlying physical dilemma must be resolved in some way by all "real-time" pitch changing devices; in most cases, this involves some form of splicing of the pitch changed signal. A number of schemes have been devised to perform this splicing; from "crummy and cheap" to "sophisticated and expensive". Our research has shown that the effectiveness of any splicing scheme (or splicing ALGORITHM) is highly program dependent. In general, an algorithm optimized for one class of signals (baroque music, for instance) will probably not work well on a different type of signal (e.g. speech).

For this reason, two different splicing ALGORITHMS are available allowing the user to select the more effective in any given application. Both of the algorithms are based on splicing between two independently read, pitch changed signals designated OUTA and OUTB.

The pitch ratio of the 949 is determined by the rate at which data are read from the memory. The "write-data" rate is fixed and equal to the SAMPLING RATE, 41kHz. To achieve a three octave pitch change range, (two octaves down, one octave up), the "read-data" rate must vary from one-quarter to twice the "write-data" rate, that is, from 10.25kHz to 82kHz. The actual read-data rate of the 949 must be double these values (20.5kHz to 164kHz) because two pitch changed outputs are required.

A large portion of the circuitry of the 949 is dedicated to providing the user with a wide range of controllable pitch change effects. All MAIN OUTPUT functions with the exception of the DELAY mode employ the pitch change capabilities of the 949. The degree of pitch change, equivalent to the PITCH RATIO, can be controlled from one of four sources; the front panel MANUAL control, an external KEYBOARD control (keyboard frequency range 1.28kHz to 5.12kHz for pitch ratios from .5 to 2), CV+MAN (an external control voltage summed with the MANUAL control), or (optionally) an intelligent remote controller (IEEE-488 bus).

READ FIFO CLOCK SELECT

The clock signal which actually reads data from the FIFO ARRAY (and determines the pitch ratio) is designated the RDFIFO clock. The FUNCTION SELECT and CONTROL MODE SWITCHES determine whether the voltage-controlled oscillator (VCO), the single side band generator (SSB), the system clock (FSYS), or an external frequency source (KYBD) reads the FIFO ARRAY.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

The VCO output is selected when in the NORMAL, EXTEND, REVERSE or DELAY mode. In the DELAY mode, the VCO has no effect on the output signal but is selected for PITCH RATIO indication, allowing the user to set the pitch ratio before switching to the pitch change mode. IC21 is a linear VCO biased to vary from 10.25kHz to 82kHz for an input voltage range of +1 to +10 volts. Phase-locked-loop IC14 and binary counter IC17 form a "frequency doubler" which multiplies the VCO output frequency by 2. This results in the desired frequency range, 20.5kHz to 164kHz. Trimpot MAXF can be used to vary the oscillator's maximum frequency (see ALIGNMENT).

The VCO can be controlled from the following sources:

1: MANUAL - The DC output (-15 to +12 volts) of the linear, front panel 10k ohm potentiometer is attenuated by an inverting op-amp (1/4 of IC22) and offset by a summing amp (1/4 IC22), resulting in a voltage range from +1 to +10 volts. In the MANUAL control mode this voltage is selected by analog switches IC's 25 and 37 and applied to the VCO.

2: CV+MAN - This mode allows an external control voltage, connected at the rear panel terminal strip, to be added to the MANUAL control. Inverting op-amp, IC22, and a pair of 50k trimpots allow a wide range of control voltages to be accommodated. Trimpot ECV LEVEL varies the gain of the op amp allowing a small control voltage range to vary the pitch ratio over a wide range or alternately, a large control voltage range can be made to control pitch over a limited range. Trimpot ECV OFFSET allows the center of the external control voltage range to be varied. The trimpots are factory adjusted so that an external control voltage of from 0 to +12 volts results in a two octave variation of pitch ratio centered about the MANUAL control setting. (See ALIGNMENT for details.)

3: KEYBOARD - The preferred means of externally controlling the pitch ratio is by an external oscillator with a frequency range of 1.28kHz to 5.12kHz. This results in a two octave pitch change range, -1/+1. In this control mode, the VCO is phase-locked to the external oscillator frequency resulting in precise pitch control with excellent long-term stability (providing, of course, that the external control frequency is stable). The KEYBOARD mode allows the pitch to be changed by precise musical intervals (25 notes over a two octave range), and is particularly useful for generating harmonies. Any keyboard instrument can be used to control the 949 if it meets the following requirements:

a) The instrument must have a continuous output when a key is depressed
b) The output frequency must vary from 1.28kHz to 5.12kHz.
c) The waveform must have at least a 3 volt peak-to-peak swing
d) The signal must be a "simple" waveform, e.g. sine, triangle or square wave.

Ideally, the external frequency is generated by an EVENTIDE HK940 KEYBOARD. This keyboard controller assures ABSOLUTE stability by synchronizing to the 949's system clock. It also features a GLIDE (portamento) control, a LOCK-mode, which maintains the pitch-ratio of the last key pressed, and the ability to control up to three 949's independently and simultaneously.

When the KEYBOARD mode is selected, the VCO becomes part of a phase-locked-loop which locks to the external KYBD INPUT frequency. This external signal is AC coupled to comparator IC9 whose square-wave output is one input to phase comparator IC15. The other input to the phase comparator is the VCO output frequency divided by 8 from IC16. The phase comparator output is low-pass filtered by the loop filter, comprised of one half of IC13. This results in the VCO running at precisely eight times the keyboard input frequency. When used with an EVENTIDE HK940 keyboard the time constant of the "frequency doubler" described above may be varied by the GLIDE potentiometer.

's 30 and 31 implement an important feature of the keyboard mode by detecting the absence of a keyboard input signal, such as when the keyboard is an organ or synthesizer and no keys are depressed. In this case, the pitch ratio is instantly set to unity (no delay change) by causing analog switch IC19 to select the system clock FSYS.

Apart from its function in keyboard operation, this feature is important in its own right. It allows the user to instantly "freeze" delay change in any of the pitch change modes by switching to the KYBD control mode with no keyboard input present. This is particularly useful in the FLANGE mode since it can be used to freeze the FLANGE at any stage.

REMOTE CONTROL VOLTAGE - Analog switch IC25 allows the pitch ratio to be OPTIONALLY varied by an intelligent controller interfaced to the standard IEEE-488 bus.

SINGLE SIDE BAND GENERATOR - SSB

The SSB is selected in the uPC, FLANGE and RANDOM modes where stable, precise control of small pitch variations is desired. The circuitry of the SSB can be divided into three sub-sections: a pair of amplitude modulators, the carrier frequency generator, and the quadrature oscillator.

An amplitude modulator is a device which multiplies two analog signals. As per convention the higher frequency signal is called the CARRIER and the lower frequency signal the MODULATION. Theoretically if the carrier and modulation inputs are sine waves, the output will be the sum of two sine waves, one whose frequency is equal to the sum of the two input frequencies (CAR+MOD) and the other's equal to the difference of the input frequencies (CAR-MOD). These two signals are called the UPPER and LOWER SIDEBANDS.

If two such modulators are connected so that the carrier inputs are of the same frequency but 90 degrees out of phase (in quadrature) and the modulation inputs are also in quadrature, then adding the two modulator outputs will yield only one sideband; either UPPER SIDE BAND (CAR+MOD) or LOWER SIDE BAND (CAR-MOD).

In the 949 the CARRIER input is FSYS (=82kHz) and the modulation is the output of a voltage controlled quadrature oscillator which can be varied from approx. 50Hz to 2000Hz.

MODULATORS: IC's 38 and 39 are monolithic modulators which will accept an AC-coupled carrier input and an AC-coupled modulation input and generate a suppressed-carrier, sum and difference frequency, output signal. Trimpots SSB1 and SSB2 can be adjusted to null the carrier component at the SSB output. (This adjustment should not be attempted without a spectrum analyzer; for details see ALIGNMENT). Each modulator has differential open-collector outputs which are cross-coupled and connected to the input of a difference amplifier (1/4 of IC41). This amplifier's output is band-pass filtered (1/4 of IC41) to remove spurious harmonics which are the result of the modulation process. The SSB signal is converted to a square wave by comparator IC18.

CARRIER FREQUENCY GENERATION: The carrier frequency of the SSB generator is derived from PC2, the 1.64MHz output of the uPROGRAM COUNTER located on the upper p.c.board, which is routed thru connector D3 (pin6). This TTL level signal is biased to drive IC44, a decoded output decade counter. Two of the ten 164kHz outputs, which are 180 degrees out of phase, drive dual data flip-flop IC42, each half of which is connected as a "toggle" flip-flop. The outputs of these flip-flops are a pair of 82kHz square waves which are 90 degrees out of phase. The output of one flip-flop, CARRIER 2, is applied to modulator IC39, while one of the two complementary outputs of the other flip-flop, CARRIER 1, is selected by a pair of analog switches, two quarters of IC43. Depending on which switch is turned on, CARRIER 1 will either LEAD or LAG CARRIER 2 by 90 degrees; which causes the SSB to generate either the UPPER or LOWER side band. Selecting the UPPER side band assures that the pitch ratio will be greater than unity while selecting the LOWER side band guarantees a pitch ratio lower than unity. One half of dual flip-flop IC46 determines which of the switches is selected. The flip-flop's state depends on a number of conditions, in particular the selected FUNCTION .

On "power-on" this circuit is synchronized by a pair of RC time constants which reset the decade counter IC44 and the dual flip-flop IC42. To insure proper sequencing the time constant of the counter is an order of magnitude greater than that of the flip-flops. It is possible, by switching the unit on and off rapidly, to throw this circuit "out of synch" rendering all SSB functions inoperative. To re-synch, turn the unit off for 10 seconds before re-applying power.

If either of the uPC (micro-pitch change) FUNCTIONS is selected, the appropriate switch of IC43 is enabled bringing one input of a pair of comparators, (1/2 of IC47), to either +12 or approx. +1 volts. This enables the appropriate comparator output which in turn sets or resets IC46 causing the SSB to generate the UPPER side band for uPC# and the LOWER for uPCb.

In the FLANGE mode, the objective is to switch alternately between UPPER and LOWER side bands thereby sweeping the delay back and forth between two "fixed" delay times. These fixed delay times are determined by a resistive, voltage-divider network which feeds an approx. +3 volt signal to one comparator and an approx. +7 volt signal to the other. With both switches of IC43 turned off the remaining input of each comparator is an analog equivalent of the CPU POINTER register from the upper p.c. board. This voltage is an accurate, linear indication of the current delay of the pitch change signal. The POINTER voltage swing in pitch change modes is normally 0 to 10 volts (0 to 25 msec respectively). In FLANGE, the comparators restrict this range to +3 to +7 volts (corresponding to a delay of approx. 7.5 to 17.5 msec), by switching to the UPPER side band (decrease delay) whenever the POINTER voltage exceeds +7 volts and the LOWER side band (increase delay) if it is less than +3 volts.

Flanging is created by adding a pitch changed (varying delay) signal and a fixed delay signal. In the FLANGE mode, the 949 automatically adds a fixed delay signal (12.5 msec) to the pitch changed signal (whose delay varies from approx. 7.5 to 17.5 msec).

In the RANDOM mode, analog switch IC45 is turned on, changing the fixed voltages at the comparator inputs to approx. +1 and approx. +9 volts, constraining the delay change to between 2.5 and 22.5 msec. Within this 20 msec range the delay is free to change according to the state of flip-flop IC46. If the flip-flop is neither being set nor reset by the comparators, then its state is dependent on PRN; the output of a digital, pseudo random noise generator. This means that, providing the delay is within the allowed range, there is a 50% probability that the delay will be increasing or decreasing, resulting in a natural, "random-walk" through the allowable delay range. If the delay exceeds either delay limit, the comparator sets (or resets) IC46 forcing the delay away from the limit.

VOLTAGE CONTROLLED QUADRATURE OSCILLATOR

Two integrating amplifiers (1/2 of IC41) connected with positive feedback, oscillate at a frequency determined by their associated RC time constants. This type of oscillator is called a "quadrature oscillator" because the outputs of the two amplifiers are sine waves which are 90 degrees out of phase. These quadrature sine waves are the modulation inputs to the modulator IC's. Three analog switches (3/4 of IC40) are employed as the voltage-controlled variable "resistors". Actually it is the average resistance of the analog switch which is varied by controlling the duty cycle of a high frequency control signal. The wider the pulse width, the lower the average resistance; with a 100% duty cycle the switch is always on and the resistance is approx. 100 ohms. At the other extreme, 0% duty cycle, the switch is always off and the resistance is approx. 1M ohm.

Comparator IC47 generates the switch control signal with a pulse width proportional to the control voltage output from op-amp IC22 (0 to +10 volt range). The control voltage is compared to a triangle waveform which is generated by low-pass filtering the square wave output of IC22. The source of this control voltage can be either the MAN, MAN + CV, or with the optional REMOTE interface card installed, a REMOTE control voltage. The KEYBOARD has no effect in any of the SSB modes

In the two uPC modes, a pair of analog switches (1/2 of IC45) are turned on and the quadrature oscillator varies from approx. 20Hz to approx. 6kHz, resulting in pitch ratios from unity to approx. .93 in uPCb and from unity to approx. 1.07 in uPC# . In FLANGE or RANDOM the switches (IC45) are turned off and the frequency is variable from approx. 20Hz to approx. 600Hz, for a pitch ratio from approx. .993 to 1.007.

PSEUDO RANDOM NOISE GENERATOR

When the RANDOM FUNCTION is selected a digital pseudo random noise generator is clocked at 820Hz (signal FSYS divided by 100, IC's 48 & 50) outputting digital noise signal PRN. PRN is the input to 1/2 of IC46, a dual data flip-flop, which controls the SSB modulator selecting pitch ratios above or below unity (decreasing or increasing delay). The noise generator is a 19 bit maximal-length shift register comprised of IC26, an 18 stage shift register, and the second half of flip-flop IC46 connected in series. Two of the outputs are fed back to the input thru XOR gate IC20.
The shift register can "latch up" if all the outputs are at zero. IC23, a seven stage binary counter, detects the "all-zero" condition and sets the flip-flop thereby re-initiating the sequence.

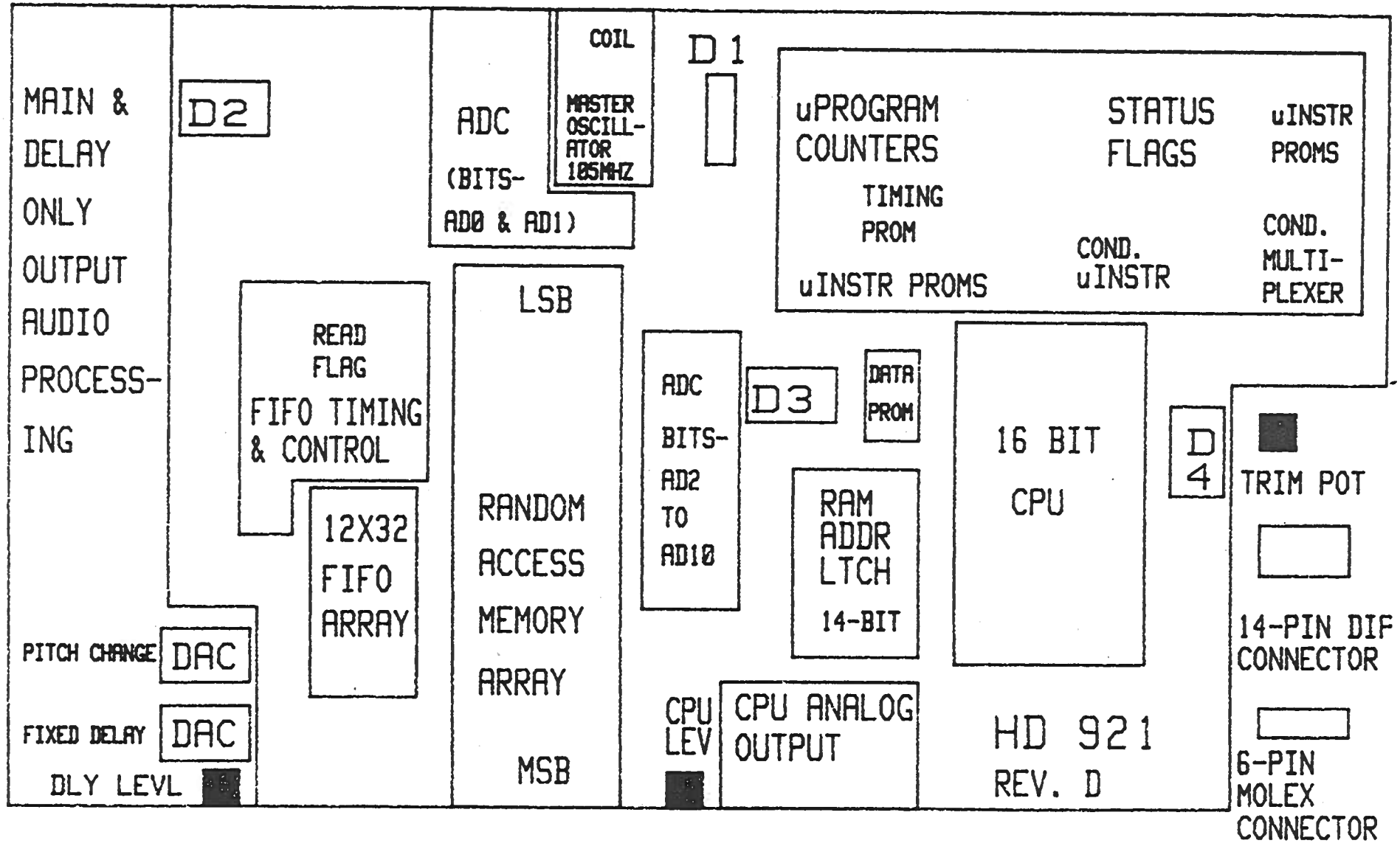
TAPE CAPSTAN DRIVE

This circuitry is designed to allow a variable speed tape machine to be controlled by the 949 in such a way that for unity pitch ratio the tape speed is normal, while ratios above or below unity will result in tape speeds slower or faster than normal. The result of this "reciprocal" control of pitch/speed is that normal pitch is maintained while the tempo is varied. This is a handy feature when trying to fit a 62 second commercial into a 60 second time slot.

1/2 of IC34, a dual monostable multivibrator and 1/4 of IC36, a quad op-amp, convert the RDFIFO clock frequency (which determines the pitch ratio) to a DC voltage. This voltage is then multiplied by the CAPSTAN DRIVE frequency, the output of VCO IC35, using the second half of IC34 and analog switch IC37. The resulting voltage is the input to the VCO. The VCO output frequency is calibrated using trimpot CAP CAL, to output a standard capstan drive frequency of 19.2kHz with the pitch ratio set to unity (see ALIIGNMENT). IC's 32 and 33 are counters which divide the VCO output down to the two other frequency standards 9.6kHz and 60 Hz. All three capstan outputs are driven by CMOS devices with a voltage swing of from 0 to 12 volts and negligible current drive capability. NOTE: DEPENDING UPON THE INPUT DRIVE REQUIREMENTS OF THE TAPE MACHINE, IT MAY BE NECESSARY TO BUFFER THE 949's CAPSTAN DRIVE OUTPUT WITH AN EXTERNAL AMPLIFIER.

AUDIO LEVEL DISPLAY

The front panel input audio indicator LEDS are controlled by the output of the ADC (analog to digital converter). IC52, a four bit binary counter, and IC 51, a four bit comparator, form an instantaneous peak hold circuit. The comparator compares the current value of the counter with the ADC outputs (four MSBs). If the ADC value is greater than the counter value, the counter is loaded (NAND gate IC49). The counter is slowly decremented so that if no peak occurs it will eventually count down. IC53, an 8 X 32 PROM, is programmed to decode the four bit counter output into the appropriate LED drive signals. One of the PROM outputs detects a count of zero and inhibits (NAND gate, IC49) further decrement pulses preventing the counter from counting thru zero. The REPEAT switch is the fifth input to the PROM. When the REPEAT switch is pushed in, LED order is reversed, indicating that the REPEAT mode is active while continuing to display an input level indication (albeit upside down).


MAIN & DELAY ONLY OUTPUT AUDIO PROCESS-ING
D2
ADC (BITS- AD0 & AD1)
COIL
MASTER OSCILL-ATOR 10.5MHZ
D1
uPROGRAM COUNTERS
TIMING PROM
uINSTR PROMS
STATUS FLAGS
COND. uINSTR
uINSTR PROMS
COND. MULTI-PLEXER
READ FLAG
FIFO TIMING & CONTROL
12X32 FIFO ARRAY
LSB
RANDOM ACCESS MEMORY ARRAY
MSB
ADC BITS- AD2 TO AD10
D3
DATA PROM
RAM ADDR LTCH 14-BIT
16 BIT CPU
D4
TRIM POT
14-PIN DIF CONNECTOR
6-PIN MOLEX CONNECTOR
PITCH CHANGE
DAC
FIXED DELAY
DAC
DLY LEVL
CPU LEV
CPU ANALOG OUTPUT
HD 921 REV. D

MASTER OSCILLATOR

Transistor Q1, a pair of 3pf capacitors and a variable inductor (located beneath the board) form a high frequency, tuned-circuit oscillator tuned to 105MHz. Transistor Q2 amplifies the oscillator output and provides the proper levels to drive TTL and ECL devices. Two dual flip-flops, IC's 29 and 30, connected in series, divide the 105 MHz signal by sixteen.

PROGRAM COUNTERS

The 6.56MHz output of IC30 drives synchronous 4-bit binary counter IC44 which outputs a 410kHz signal to IC45, a synchronous 4-bit decade counter. The 41kHz output of IC45 (pin 7) is the 949's sampling frequency. The least significant output of IC44 (pin 3), at a frequency equal to 205kHz, is the CPU clock signal CCPU. The seven most significant outputs of IC's 44 & 45 comprise an eighty count PROGRAM COUNTER with outputs designated PC1-PC7. The program counter outputs access the micro-instructions stored in the uINST proms.

TIMING PROM

Program counter outputs PC3 to PC7 are the address inputs to IC46, a 8X32 programmable read only memory (PROM). In normal operation only 20 of the 32 8-bit words are accessed (because PC4-PC7 are the outputs of a decade counter). The outputs are defined as follows:

IC 46

PIN#	NAME	DESCRIPTION
1	NSPTR	SAMPLE POINTER VOLTAGE not
2	SAMP	SAMPLE INPUT AUDIO SIGNAL
3	SELECT	ENABLE uINST PROM OUTPUTS
4	T5	uINST PROM ADDRESS BIT
5	T4	uINST PROM ADDRESS BIT
6	NRSTAD	RESET ADC not
7	NENAD	ENABLE ADC not
	SDLO	SAMPLE DELAY ONLY OUTPUT

CENTRAL PROCESSING UNIT (CPU)

The 949's sixteen-bit CPU comprises four "bit slice" bipolar IC's of four bits each, part # 2901. Each chip contains a four-bit multifunction Arithmetic Logic Unit (ALU), instruction decoding and timing logic, and sixteen four-bit general purpose registers. These registers are of the "two-port" variety which allow simultaneous READ/WRITE operations with independent read/write addresses or simultaneous reads from different addresses. The 2901 also provides zero and sign status outputs.

The four 2901's, IC's 22-25, are connected to form the 16-bit CPU with IC22 being the most significant slice (MSS). The ten microinstruction inputs (I9-I0,CO) as well as the eight address lines (four A-port, four B-port address bits) are connected in parallel across all four slices. Sixteen-bit data is input to the CPU on the "D-bus" and sixteen-bit output data are output on the "Y-bus".

MICRO-INSTRUCTION (uINST) PROMS

Every sample period (approx. 25 usec) a sequence of eighty micro-instructions (uINST) is accessed by program counter outputs PC1-PC7. These uINST's are stored in eight 8X32 PROM's organized as four pairs of PROM's with the corresponding outputs of each pair connected together. This forms, in effect, a single 32X64 PROM, four PROM's wide and two PROM's deep. In this way, program storage is divided into two sections of four PROM's each. TIMING PROM bit SELECT and 1/6th of inverter IC31 enable the TRI-STATE outputs of first one group of four PROM's and then the other. IC's 47, 49, 51 and 60 store micro-instructions for the first 32 program steps and IC's 48, 50, 52 and 61 store steps 32-79. The 48 program steps 32-79 are read from the 32 bit proms by accessing 16 of the PROM addresses twice. TIMING PROM bits T4 and T5 are the two most significant address bits of the second group of PROM's. These address bits select one of four groups of eight PROM addresses. This scheme allows groups of eight micro-instructions each (sub-routines) to be repeated. The uINST PROM output designations are as follows:

IC49 & IC50

PIN#	NAME	DESCRIPTION
1	I8	CPU uINST bit
2	I0	CPU uINST bit
3	I1	CPU uINST bit
4	B0	CPU B-port addr bit
5	B1	CPU B-port addr bit
6	B3	CPU B-port addr bit
7	I4	CPU uINST bit
9	I5	CPU uINST bit

IC51 & IC52

PIN#	NAME	DESCRIPTION
1	A3	CPU A-port addr bit
2	A1	CPU A-port addr bit
3	A0	CPU A-port addr bit
4	I6	CPU uINST bit
5	CI7	COND'L uINST bit
6	CC0	COND'L CPU CARRY IN
7	CA2	COND'L A-port addr
9	I2	CPU uINST bit

IC60

1	CI3	COND'L uINST bit
2	CKRMP	Clock RAMP FLAG
3	CKDIR	Clock DIRECTION FLAG
4	CB2	COND'L B-port addr bit
5	X7C	I7 MULTIPLEXER addr bit
6	X7B	"
7	X7A	"
9	X3A	I3 MULTIPLEXER addr bit

IC61

1	CI3	COND'L uINST bit
2	-	UNUSED
3	XB2	ENABLE COND'L B2
4	CB2	COND'L B-port addr bit
5	X7C	I7 MULTIPLEXER addr bit
6	X7B	"
7	X7A	"
9	X3A	I3 MULTIPLEXER addr bit

IC47

1	-	UNUSED
2	X3B	I3 MULTIPLEXER addr bit
3	NWRT	RAM ARRAY WRITE NOT
4	XA2	ENABLE COND'L A2
5	SFXD	SAMPLE FIXED DELAY
6	MAC	RAM ARRAY ACCESS
7	CKSN	Clock SIGN FLAG
9	CKZR	Clock ZERO FLAG

IC48

1	X3B	I3 MULTIPLEXER addr bit
2	X3C	"
3	CKDAC	CPU OUT to DAC LATCH
4	SREF	SAMPLE MAIN OUT REF
5	CKFIFO	LOAD FIFO ARRAY
6	MAC	RAM ARRAY ACCESS
7	CKSN	Clock SIGN FLAG
9	CKZR	Clock ZERO FLAG

CONDITIONAL MICRO-INSTRUCTIONS

The MICRO-PROGRAM of the 949 can execute a limited type and number of conditional micro-instructions by inverting the status of up to 3 bits of the CPU uINST word (bits I3, I7 and C0) if a specified condition is true.

CONDITIONAL uINST bit I7:
With I8=0, the status of I7 determines whether or not the result of the current CPU operation is stored in the register specified by the B-port address. If I7=0 the result is not stored.

Conditional uINST bit CI7 (IC's 51 & 52) is one input to an exclusive-or (XOR) gate IC53 whose output is CPU uINST bit I7. The other input of the XOR gate is the output of an eight-in one-out multiplexer IC62. One of the 8 multiplexer inputs is selected by the three-bit address XI7 (uINST bits X7C, X7B, X7A). For unconditional instructions XI7=0 which selects input 0 of IC62. Since input 0 is connected to ground, the XOR gate passes CI7 unchanged (I7=CI7). Selecting one of the other multiplexer inputs will cause the XOR gate to invert CI7, (I7=NOT(CI7)), if the selected input is true. The multiplexer input assignments are listed below:

CONDITIONAL uINST bits I3 & C0:
The CPU uINST bits can be conditionally inverted in the same manner as described above for I7. Conditional uINST bit CI3 is one input of XOR gate IC56. The other XOR input is the output of eight-in one-out multiplexer IC63. One of the 8 multiplexer inputs is selected by three-bit address XI3 (uINST bits X3C, X3B and X3A). For unconditional instructions XI3 can be either 0 or 7 as these inputs are connected to ground. Selecting one of these inputs will cause the XOR gate to pass CI3 unchanged (I3=CI3). Selecting one of the remaining inputs will cause the XOR gate to invert CI3 (I3=NOT(CI3)) if the selected input is true.

Inverting uINST bit I3 changes an addition operation to subtraction, a pass operation to an invert, etc. To satisfy the requirements of the binary number system used by the CPU, the input carry bit C0 must be 0 for addition and 1 for subtraction. For this reason, conditional uINST bit CC0 is applied to XOR gate IC53 and conditionally inverted by the output of multiplexer IC63.

I7 MULTIPLEXER----IC 62

PIN#	INPUT	CONDITION
4	0	GROUND
5	1	ALGORITHM
2	2	NOT(RANDOM or FLANGE)
1	3	EXTEND PC
15	4	SIGN FLAG
14	5	ZERO FLAG
13	6	READ FLAG
12	7	(READ) AND (ZERO)

I3-C0 MULTIPLEXER----IC 63

PIN#	INPUT	CONDITION
4	0	GROUND
3	1	ALG1
2	2	RAMP FLAG
1	3	PC7
15	4	NOT REVERSE
14	5	DIR FLAG
13	6	SIGN FLAG
12	7	GROUND

CONDITIONAL CPU REGISTER ADDRESSES

Both A and B port CPU registers can be conditionally addressed to a limited extent. XOR gate IC53 allows uINST bit A2, (one of four A-port address bits), to be inverted if both program counter bit PC7 and uINST bit XA2 are true. XOR gate IC56 performs an identical function on uINST bit B2 (with qualifier uINST bit XB2). This conditional addressing scheme allows the same uINST to be executed more than once using different source and destination registers each time.

STATUS FLAGS

The 949's micro-program employs five status flags as conditional micro-instruction qualifiers. Two of these flags, ZERO and SIGN, store the status of CPU operations while the three remaining flags, RAMP, DIR and READ, indicate pitch change status.

ZERO FLAG - 1/2 of dual data latch IC54 is strobed by uINST bit CKZR. When strobed the flag is set to 1 if the current CPU output is equal to zero.

SIGN FLAG - 1/2 of dual data latch IC54 is strobed by uINST bit CKSN. When strobed the flag is set to 1 if the current CPU output is negative.

RAMP FLAG - 1/2 of dual data latch IC55 is strobed by uINST bit CKRMP. The RAMP FLAG initiates ALGORITM 2 splicing ramps and is a convenient oscilloscope trigger point for observing ALGORITHM 2's splicing operation.

DIR FLAG - 1/2 of dual data latch IC55 is strobed by uINST bit CKDIR. The DIR FLAG indicates the direction of delay change (pitch ratio increasing or decreasing). In all pitch change modes the DIR FLAG is set to 1 if the pitch ratio is greater than unity (delay decreasing) and 0 if less than unity (delay increasing). If the pitch ratio is precisely unity (delay not changing) the DIR FLAG's status indicates the direction of t last delay change. The DIR FLAG is an important diagnostic aid in that its proper operation indicates that a significant portion of the CPU and associated circuitry is functioning properly. NOTE: In all of the pitch change modes, delay change can be stopped by selecting the front panel KYBD CONTROL MODE and disconnecting any control frequency input such as the keyboard.

READ FLAG - 1/2 of dual data latch IC13 is strobed every sample period storing the FIFO ARRAY's status. The READ FLAG indicates that the FIFO ARRAY is half empty and requests a transfer of four data words from RAM to FIFO.

CPU DATA INPUT

The sixteen-bit CPU data input bus is referred to as the "D-bus". The DATA PROM IC43 inputs necessary 8-bit program constants to the CPU on lines D7-D14. The most significant input bit D15 is grounded and the 7 least significant bits D0-D6 are pulled-up to +5 volts by a 100k resistor network. Since IC43 is a 8X32 bit PROM it cannot output a unique constant value for each program step, instead a unique value is ailable for each consecutive group of four instructions. The DATA PROM's TRI-STATE outputs are disabled twice every sample period allowing MAIN and DELAY ONLY delay set data to be input to the CPU.

CPU ANALOG OUTPUT

The eight least significant bits of the CPU, Y0-Y7, are stored when uINST bit CKDAC strobes eight-bit latch IC38. IC's 36 & 37 convert the 8-bit latch output to an analog voltage designated CPU ANALOG OUT.

Three independent analog signals are generated by the CPU each sampling period; two splicing signals REFA & REFB (reference voltage inputs of the MAIN OUTPUT DAC) and a voltage corresponding to the current value of the pitch-change POINTER register. In all three cases, the voltage swing is 0 to 10 volts. In the case of the pointer voltage an output of 0 volts corresponds to 0 delay while a 10 volt output corresponds to a delay of 25msec.

11X16K DYNAMIC RAM ARRAY

Eleven 16K dynamic random access memory (RAM) IC's, M0-M10, comprise the digital audio data storage of the 949. The seven address inputs, row address strobe (NRAS), column address strobe (NCAS), write (NWRT), as well as the three power supply lines (+12, +5 and -5 volts), are connected in parallel across all eleven RAMS. NWRT goes low once per sample period to write new data into the base address location. When the REPEAT switch is depressed NWRT is disabled and no new data is written into memory.

The data inputs to the RAM are the outputs of the analog-to-digital converter (ADC) counters. The RAM ARRAY outputs data to the DELAY ONLY OUTPUT DAC and the 12X32 FIFO array.

ANALOG-TO-DIGITAL CONVERTER (ADC)

Every sample period the pulse-width modulated representation of the audio signal is converted to an eleven-bit binary word. This is accomplished as follows:
The pulse-width modulated audio signal, CMP, from HA931 via connector D2, is one input to IC26, a two input NAND gate. The second NAND gate input is TIMING PROM output NENAD which defines the conversion period. During conversion the NAND gate enables an 11 bit binary counter chain comprised of IC's 28, 32, 33 & 34. The counter chain remains enabled until either CMP goes low or the end of conversion (NENAD). In this way, the pulse width, which is proportional to the audio signal level, determines the number of positive clock transitions (105MHz input clock) input to the counter chain and hence the resultant count. At the end of the conversion period, NWRT goes low and a random access memory (RAM) write cycle is initiated, writing the 11 bit word into the 11X16K RAM array. When the data has been stored, the ADC counters are reset by TIMING PROM output NRSTAD in preparation for the next conversion cycle. In the event that the counters overflow during conversion (count greater than 2047), the carry output of IC34 sets the overflow flag IC32. The overflow flag sets the ADC to its maximum count of 2047 by setting each bit of the counter chain high. The overflow flag is cleared when the ADC is reset by NRSTAD.

DELAY ONLY OUTPUT

Eleven-bit DELAY ONLY DAC IC9 (a twelve-bit multiplying DAC) in conjunction with one-half of quad op amp IC7, converts the RAM output to an analog voltage. The DLY LVL trim pot varies the DAC's reference voltage which in turn determines the maximum output voltage swing. The reference voltage should be adjusted to approximately -10 volts resulting in a 0 to +10 volt swing at the op amp output. FOR PROPER ADJUSTMENT REFER TO ALIGNMENT INSTRUCTIONS.

The RAM ARRAY is enabled for approx. 3usec allowing the DAC output to settle and analog switch IC6 to turn on, charging the .001uF hold capacitor. uINST bit SDLO is the sample control signal which closes the switch for approx. 1.5usec. The hold capacitor voltage is buffered by op amp IC5 which is AC coupled (removing +5 volt bias) to inverting amplifier IC1. The output of IC1 runs to connector D2 and is designated DDAC.
NOTE- The analog switches employed in the 949 can only pass signals limited to a 0 to +10 volt range. For this reason, a +5 volt D.C. bias is superimposed on signals where necessary.

FIXED DELAY OUTPUT

For the MAIN OUTPUT functions of DELAY and FLANGE the main output signal must contain a stable fixed delay. In the DELAY mode, the FIXED DELAY i[s] equal to the front panel MAIN OUTPUT DELAY SET SWITCHES. If the FLANGE mode is sele[cted], the FIXED DELAY is equal to the switch setting plus 12.5msec. The appropriate FIXED DELAY signal is applied to the sample and hold cicuitry of analog switch I[C] a .001uF capacitor and op amp IC3. This signal is input to analog switch IC2 as w[ell] as to the phase shift network of IC1. The output of this phase shift network is [a]pplied to a 2nd switch of IC2 and the switch outputs are connected together so that [either] the direct or phase-shifted FIXED DELAY signal can be selected. In DELAY [mode] the direct FIXED DELAY signal is selected, in FLANGE the phase-shift signal [is] selected, in all other modes both switches are off. The selected signal is summed [at] summing amplifier IC1, whose output is desigated MDAC at connector D2.

FIRST-IN FIRST-OUT (FIFO) REGISTERS

Six 4X16 FIFO's, IC's 16-21, are organized as a 12X32 FIFO [array]. Inputs of the FIFO inputs come from the outputs of the dynamic RAM ARRAY with [the] corresponding FIFO outputs connected to the MAIN OUTPUT DAC IC8. The READ FLA[G] IC12 requests a RAM read c[y]cle ration of the CPU whenever the FIFO is less than half f[ull] (fewer than sixteen words stored). The read from RAM and write to FIFO sequenc[e] occurs as follows:

1) The CPU computes and outputs the RAM address for the ne[xt] OUTA data word.
2) uINST bit MAC initiates a RAM read.
3) uINST bit CKFIFO gated with the READ FLAG clocks RAM OU[T] data into the FIFO
4) Steps 1 to 3 are repeated for OUTB data
5) Steps 1 to 4 are repeated.

The result of the above sequence is that if the READ FLAG [is] true for a given sample period, four data words (two for OUTA and two for OUTB) ar[e] read from RAM to FIFO.

RDFIFO from connector D2 is input to a dual monostable mul[tivibrator] IC15 which ensures that the FIFO shift-out clock's pulse width is gre[ater] than 100nsec (narrower pulses may be ignored by one or more FIFO's, resulting in [an] "OUT OF SYNCH" condition).

Data is clocked out of the FIFO and to the DAC at a rate v[arying] from 20.5kHz to 164kHz. The shift out clock is inhibited whenever the FIFO [array] is empty or the DELAY m[ode] is selected.

As described above, data shifted thru the FIFO alternately [is] a sample of OUTA and OUTB. Due to the asynchronous nature of FIFO's it is i[mpossible] to determine whether a given output word is part of output A or B. It i[s] therefore necessary to "tag" the data words so that they can be identified as bel[onging] to the A or B output. Program counter signal PC4 is used as the "tag" bit (twelf[th] data bit). PC4 is zero when OUTA words are shifted into the FIFO array and o[ne] for OUTB words.

MAIN OUTPUT DAC

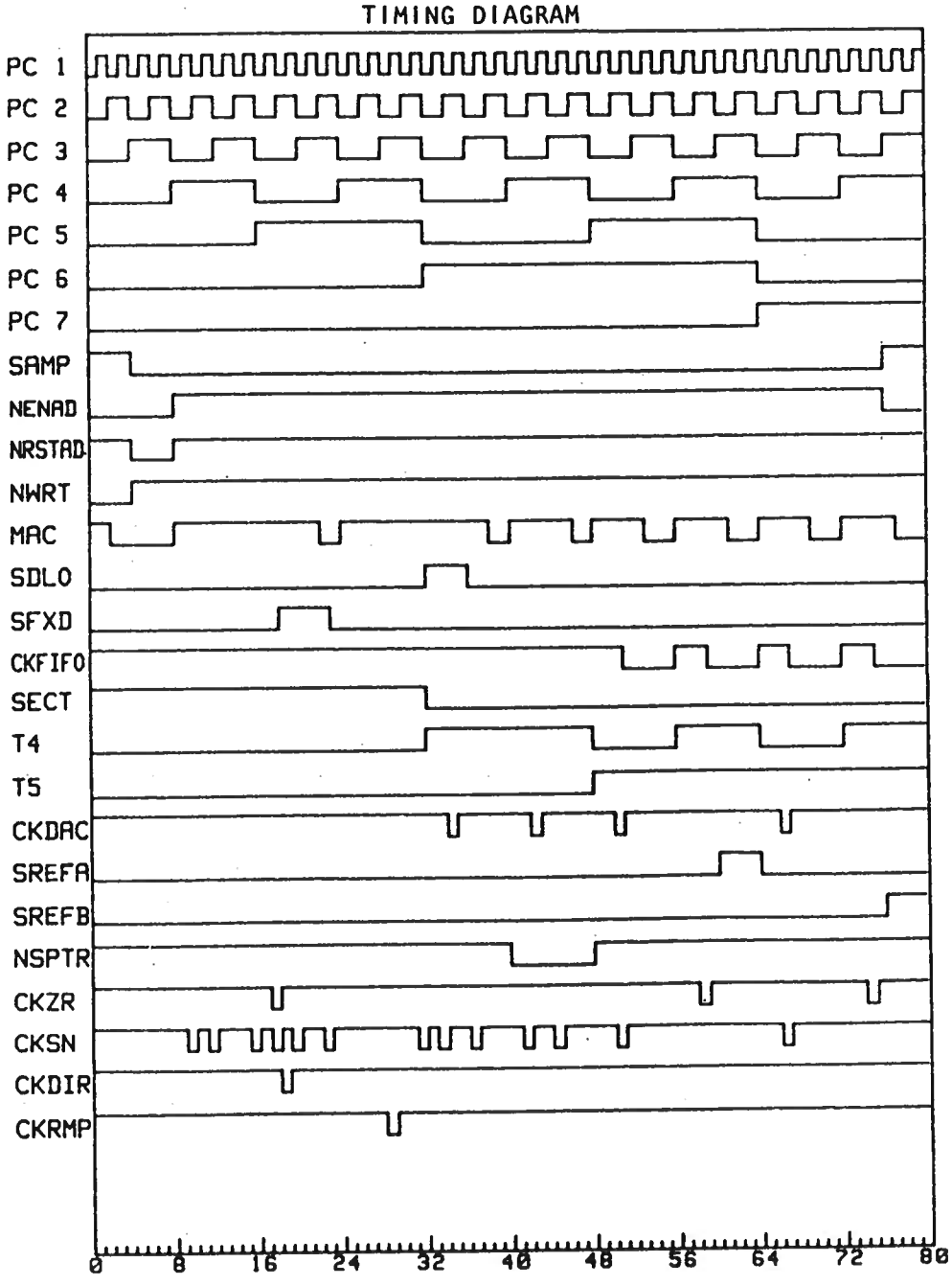
IC8, a 12-bit multiplying DAC and a pair of op amps, 1/2 o[f] IC7, convert the FIFO outputs to an analog voltage. The output of IC7 is a multi[plexed] audio signal containing alternately OUTA and OUTB data at the RDFIFO cl[ock] rate. The "tag" data bit, designated A/B at the FIFO output, is used to de-mult[iplex] the two pitch changed audio signals by appropriately gating the sample pulses of [the] two independent sample and hold cicuits. Two of the op amps of IC5 buffer the two [output] signals which are then AC coupled and summed by op amp IC1. The output of IC [is] then gated MDAC and runs to connector D2.

MAIN OUTPUT REFERENCE VOLTAGE

As mentioned previously the CPU analog output contains three multiplexed signals REFA, REFB, and POINTER. The two reference signals must be applied to the MAIN OUTPUT DAC reference input during the time slot corresponding to the proper output, OUTA or OUTB. Since the output rate of the reference signals (CPU out) is 'system synchronous and the output rate of the two pitch changed outputs is not, the CPU output must first be de-multiplexed at a synchronous clock rate and then re-multiplexed at the pitch change rate.

A pair of analog switches, 1/2 of IC4, and 1/2 of quad op-amp IC3 sample and hold the two reference voltages, REFA and REFB. The two sample pulses are generated by NORing (IC11) uINST bit SREF with PC7. REFA and REFB are then multiplexed by a pair of analog switches, 1/2 of IC2, and summing amp IC5. FIFO "tag" output A/B and its inverse N(A/B) control the switches turning on REFA when OUTA is valid and REFB when OUTB is valid at the MAIN DAC output.

TIMING DIAGRAM



HP 941 REV. D - Front Panel P.C. Board

HP 941 supports all of the front panel controls and indicators with the exception of the POWER switch and the audio LINE switch. Three 14-pin DIP connectors, designated P1 through P3, connect the front panel p.c. board to the lower p.c. board HA 931. A fourth DIP connector, D4, routes delay set information to the upper p.c. board HD921.

P1 carries +15 and -15 volts as well as all audio connections. P2 and P3 carry +5 and +12 volts, FUNCTION and CONTROL MODE select lines, REPEAT, ALGORITHM and PITCH RATIO signals.

INPUT LEVEL

The INPUT LEVEL potentiometer is routed to connector P1. The cathodes of the LED level indicators are routed to P2 through current limiting resistors while the anodes are connected to +5 volts. The REPEAT switch is a locking PUSH-ON/PUSH-OFF switch whose output is de-glitched by two of the inverters of IC6.

FEEDBACK

The outputs of the FEEDBACK LEVEL potentiometers are summed by 1/2 of op amp IC8 which drives a passive equalization network. A pair of 100k ohm log taper potentiometers vary the frequency response of the network and its output is amplified by an inverting op amp 1/2 of IC8.

DELAY SET SWITCHES

Two banks of six locking PUSH/PUSH switches allow independent delay setting of the 949's outputs. The MAIN and DELAY ONLY switch banks are strobed by timing signals SREFB and SREFA respectively. These signals are routed from connector P3 and enable IC4 (a quad analog switch) which pulls the active pole of the appropriate bank of switches to +5 volts. Corresponding outputs of the two banks of switches are OR'd together through diodes and connected to the inputs of hex TRI STATE buffer IC6 (an 80C97). The outputs of IC6, which are enabled at the proper time by NOR gate IC5, are connected to the CPU input bus via connector D4. One-quarter of analog switch IC4 disables the MAIN DELAY SET switches 6.25, 12, and 25msec. except when the MAIN OUTPUT "DELAY" FUNCTION is selected.

CTION SELECT

The MAIN OUTPUT FUNCTION is determined by the setting of five switches, one PUSH/PUSH type and a bank of four interlocking double-pole, double-throw (DPDT) switches. Each interlocking switch selects one of two functions as determined by the setting of the PUSH/PUSH FUNCTION switch. The selected function line is brought low while the remaining seven lines are pulled up to +12 volts. The eight FUNCTION SELECT outputs are routed to HA931 through connectors P2 and P3. Eight inverting buffers, IC's 5 & 6, drive the RED/GREEN FUNCTION SELECT INDICATOR LEDS. For proper operation, one, and only one, of the four interlocking switches must always be selected.

ALGORITHM SELECT

The PUSH-ON/PUSH-OFF ALGORITHM select switch determines the splicing algorithm used in the PITCH CHANGE modes (NORMAL, EXTEND, uPC, and REVERSE). ALGORITHM 1 should always be selected for pitch ratios below .5 (one octave down). In the RANDOM and FLANGE modes ALGORITHM 2 is normally selected. Selecting ALGORITHM 1 will introduce an additional delayed signal at low level, which may or may not be desirable. In the DELAY mode, the ALGORITHM switch has no effect.

CONTROL MODE SELECT

A bank of three interlocking DPDT switches selects the 949's pitch change control mode and also turns on the appropriate LED indicator. When the MANUAL control is selected, the front panel 10k linear pot controls the pitch ratio. When CV+MAN is selected the MANUAL control voltage is added to an external control voltage signal input at the rear panel terminal strip. The KEYBOARD control mode allows the pitch ratio to be controlled from an external keyboard or audio frequency oscillator (frequencies from 1.28kHz to 5.12kHz for pitch ratios from .5 to 2.00) when either the NORMAL, EXTEND or REVERSE MODE is selected.

NOTE: If the KEYBOARD CONTROL MODE is selected without applying a keyboard input signal, the PITCH RATIO is set to unity which FREEZES DELAY CHANGE. This allows delay change to be stopped at any point by pressing the KEYBOARD switch. While true in all modes, this feature is particularly useful in the FLANGE mode, allowing the user to stop the flange sweep at any point. Delay change (or flange sweep) starts again when one of the other control modes is selected.

PITCH RATIO READOUT

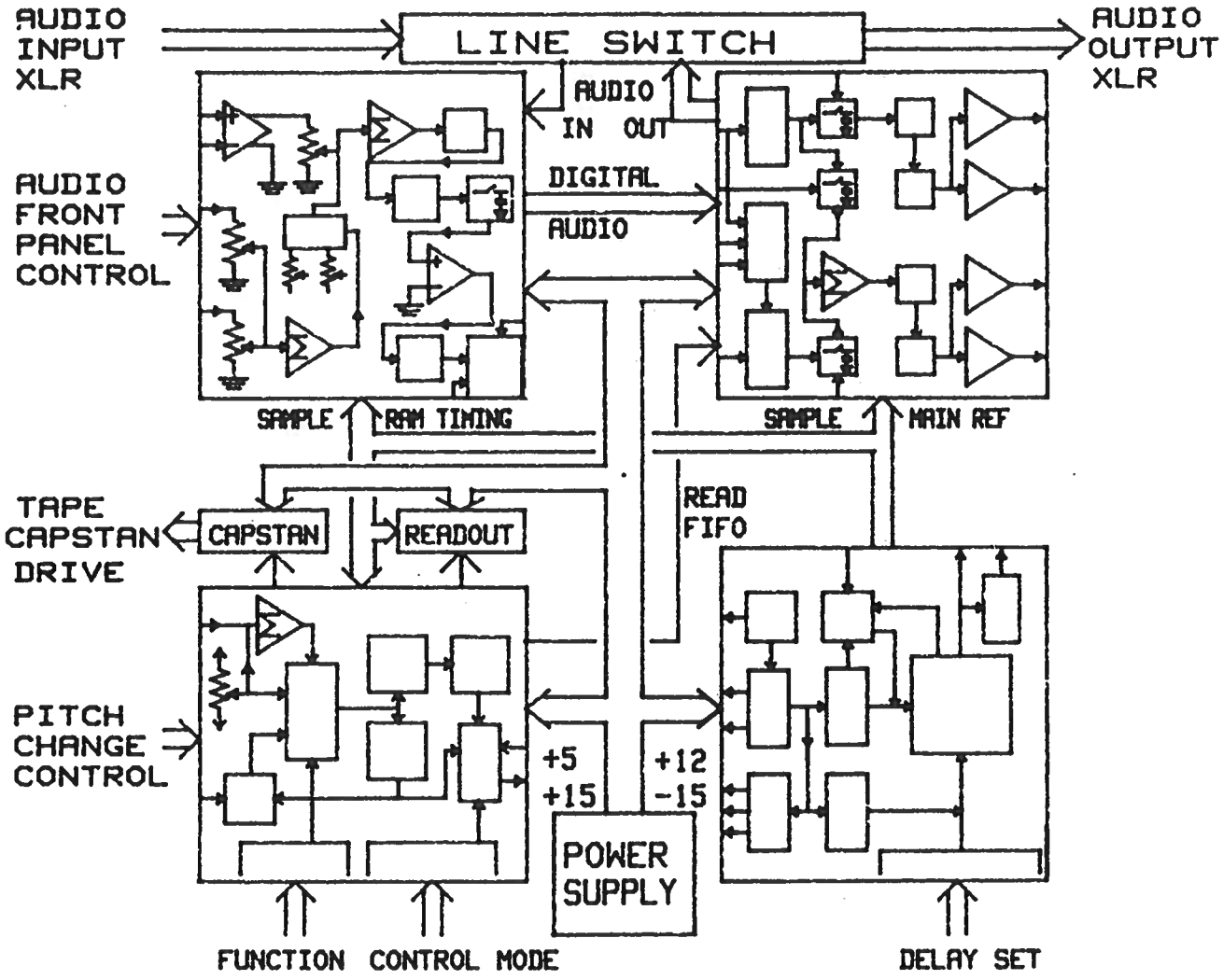
The four digit readout is driven directly by IC1, a 28 pin frequency counter/display driver I.C. A pair of dual monostable multivibrators, IC's 2 & 3, generate the following timing signals:

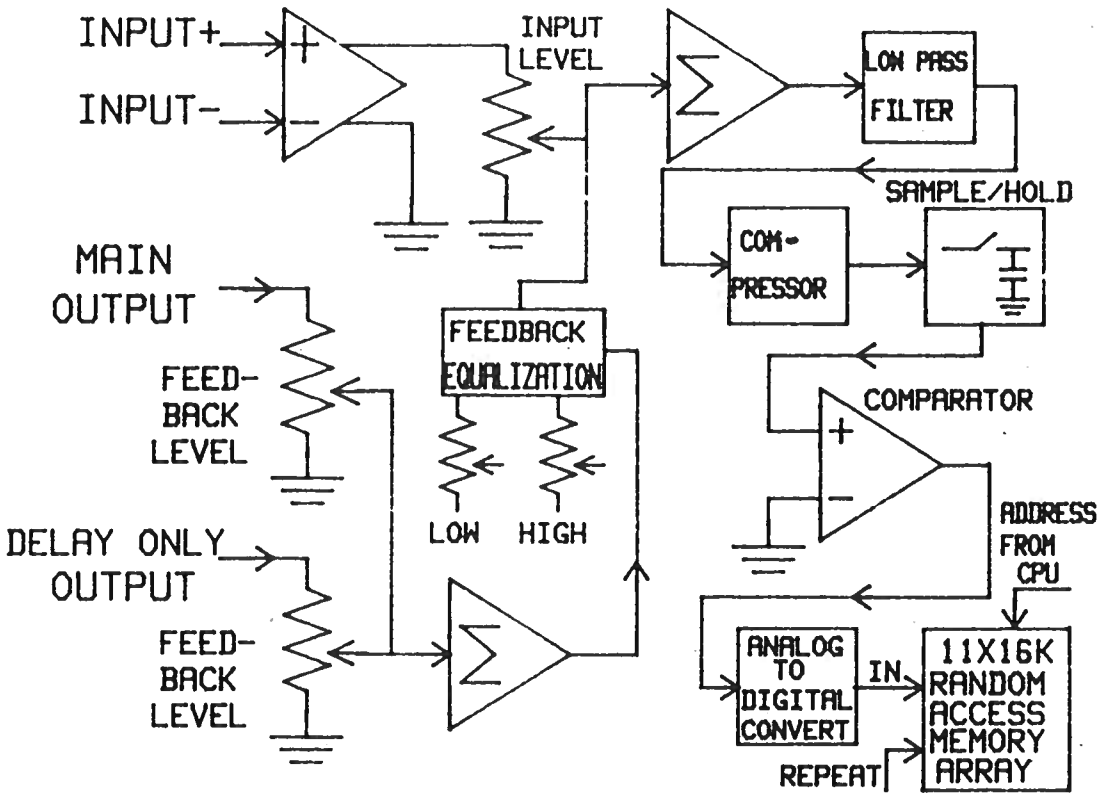
1) RESET - Resets the counter at the end of each counting period (approx. 1/10 second),
2) STORE - The store signal loads the output latches of IC1 at the end of each counting period. These latch outputs drive the LED readout.

3) COUNT - The read FIFO clock, RDFIFO, is divided by ten on HA 931 and the resulting signal FPR is connected to HP 941 via connector P2. Monostable IC2 gates FPR and outputs COUNT to IC1.

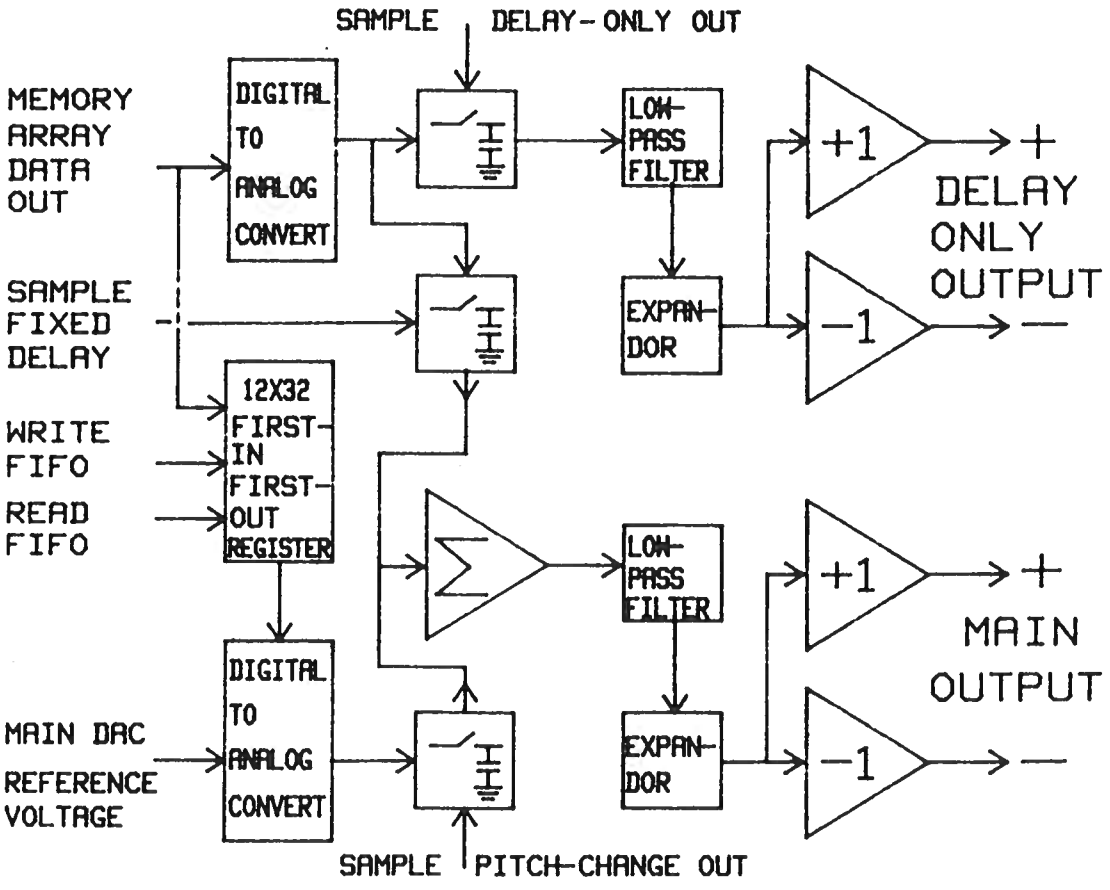
The COMMON ANODE display is multiplexed by digit drive signals D0 to D3 enabling the digits in sequence. The seven-segment drive signals SA to SG turn on the appropriate segments of each digit. One of the inverters of IC4 lights the decimal point of the most significant digit by inverting digit drive signal D3.

MASTER BLOCK DIAGRAM

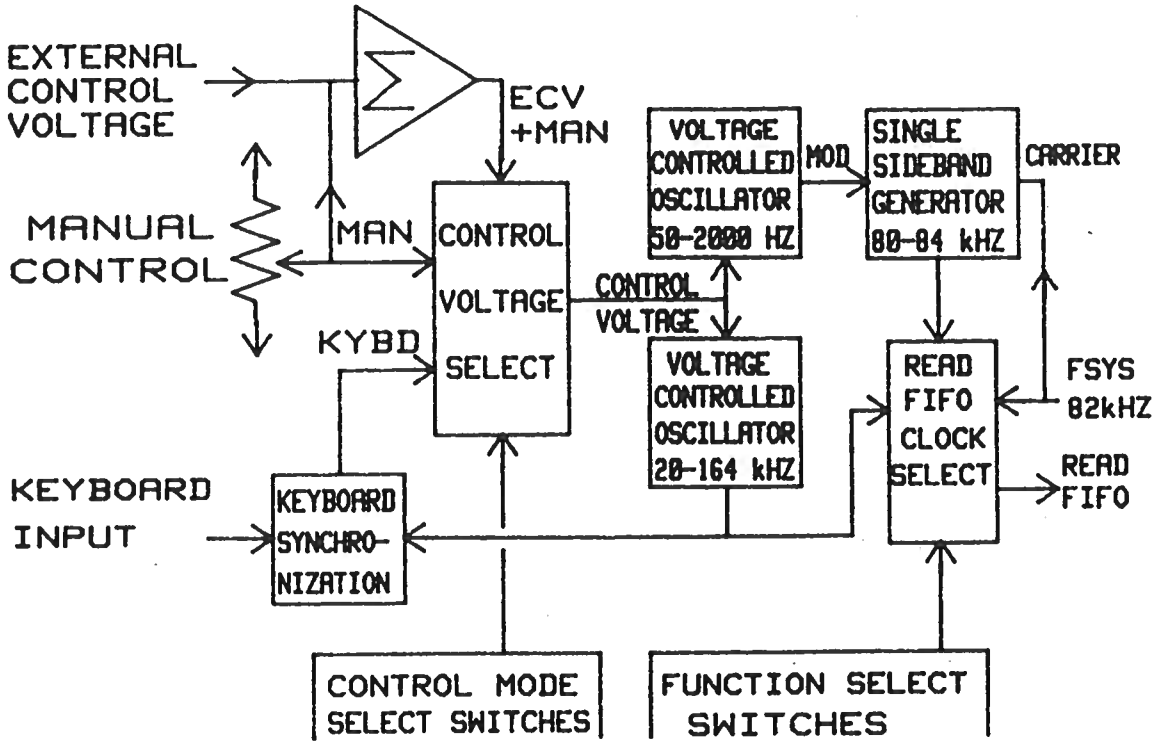




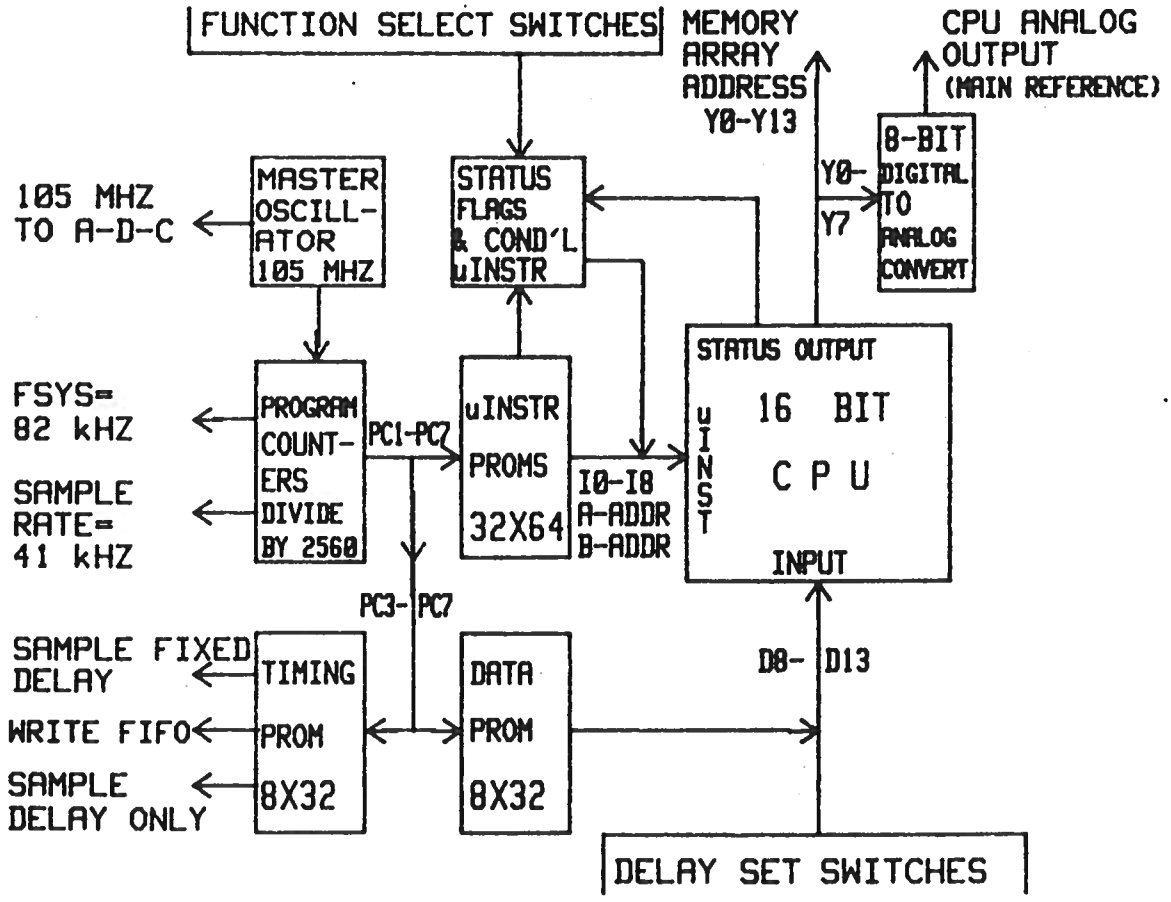
INPUT AUDIO PROCESSING



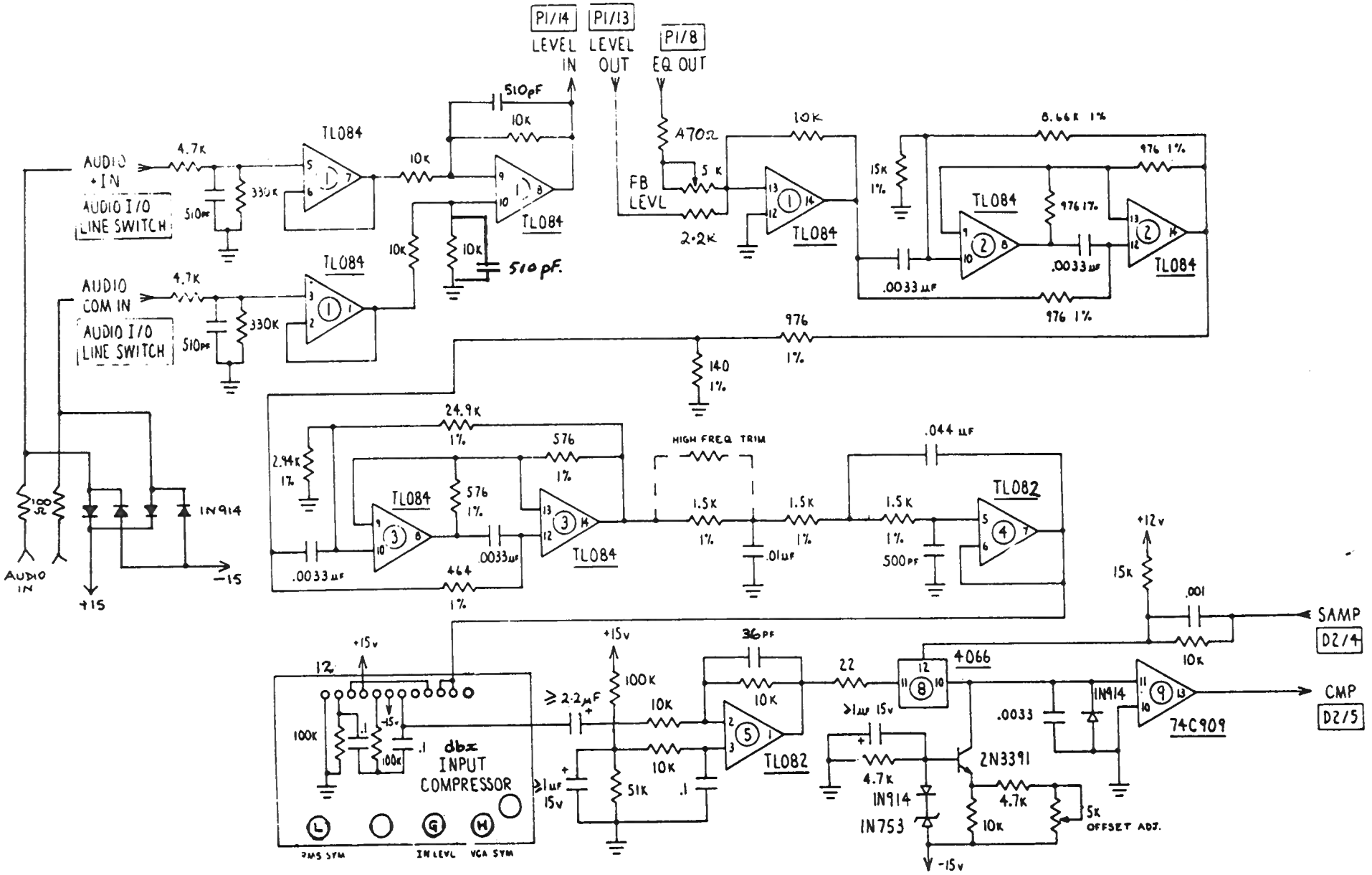
OUTPUT AUDIO PROCESSING



PITCH CHANGE TIMING & CONTROL



SYSTEM TIMING & CENTRAL PROCESSING UNIT



INPUT AUDIO PROCESSING

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SHEET 1 OF 6

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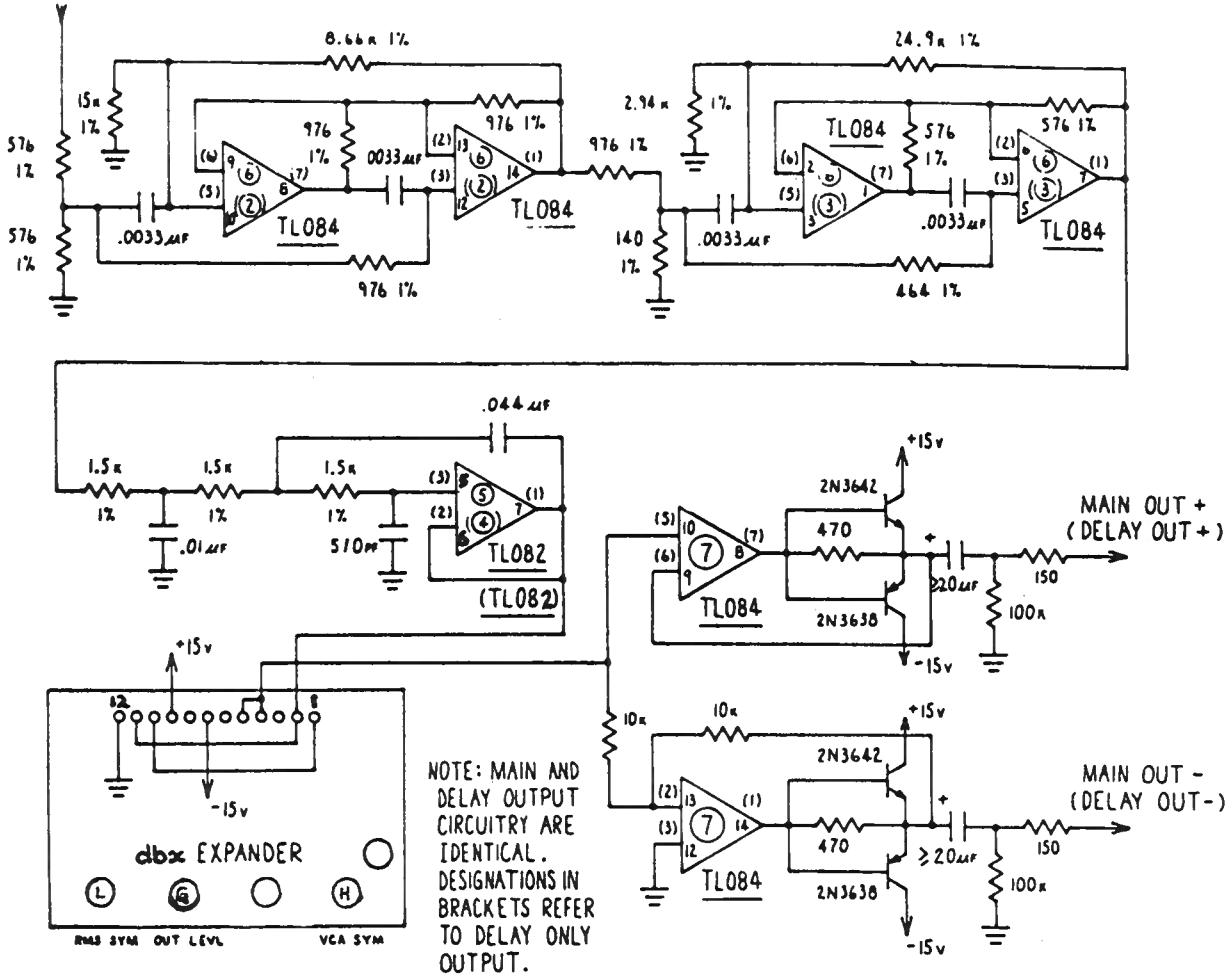
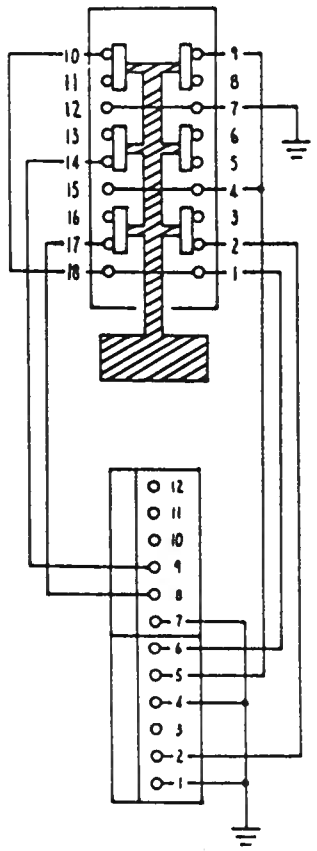
H949 page S4.

D2/14 MDAC
(2) (DDAC)



NOTE: MAIN AND DELAY OUTPUT CIRCUITRY ARE IDENTICAL. DESIGNATIONS IN BRACKETS REFER TO DELAY ONLY OUTPUT.



LINE SWITCH

6 POLE / DOUBLE THROW PUSH - PUSH SWITCH

AUDIO I/O

MOLEX SOCKET

PIN ASSIGNMENTS

PIN #	SIGNAL	
1	GND	
2	COM	DELAY ONLY XLR
3	+	DELAY ONLY XLR
4	GND	
5	+	AUDIO IN XLR
6	COM	AUDIO IN XLR
7	GND	
8	COM	MAIN OUT XLR
9	+	MAIN OUT XLR

OUTPUT AUDIO PROCESSING

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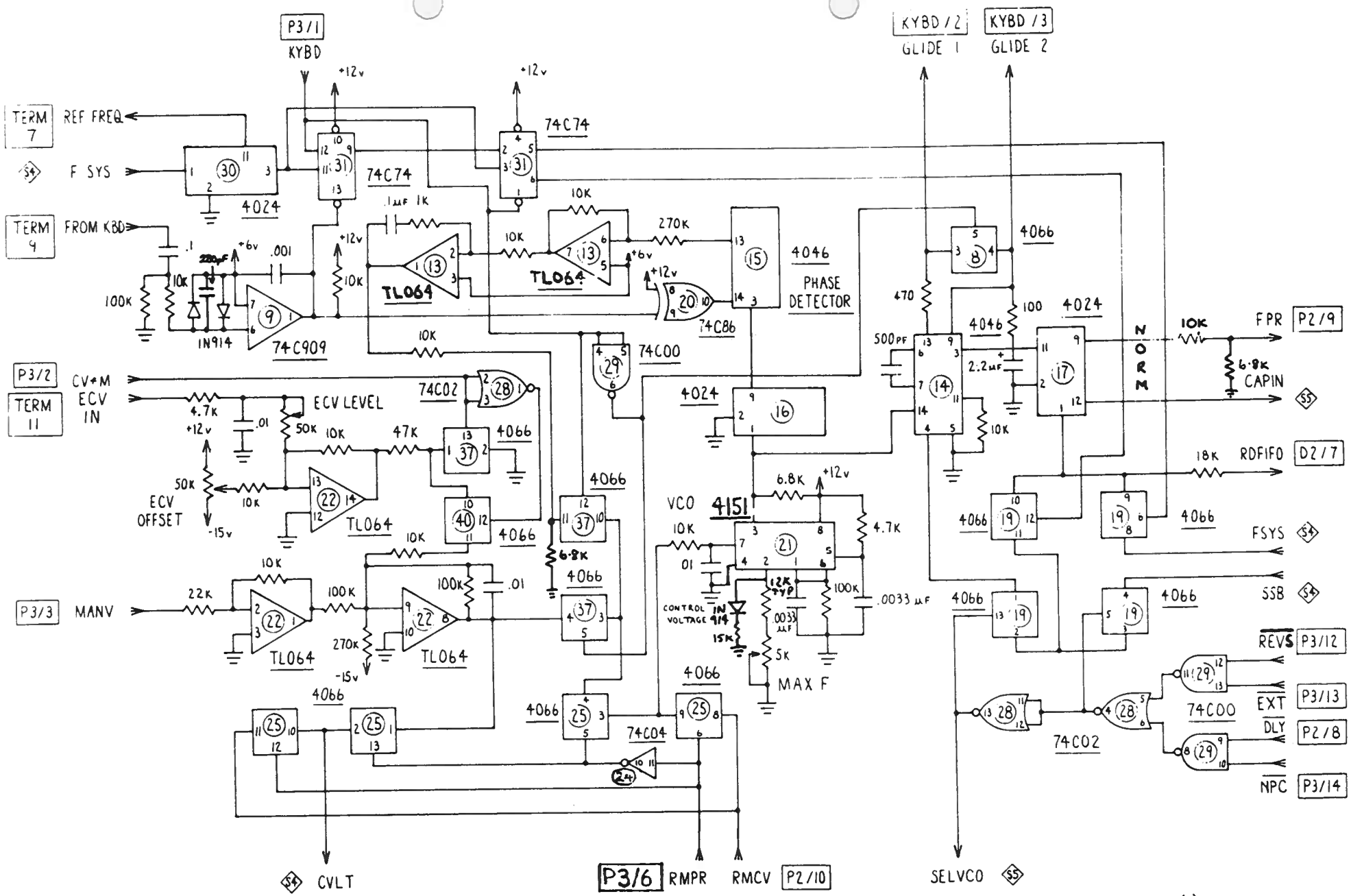
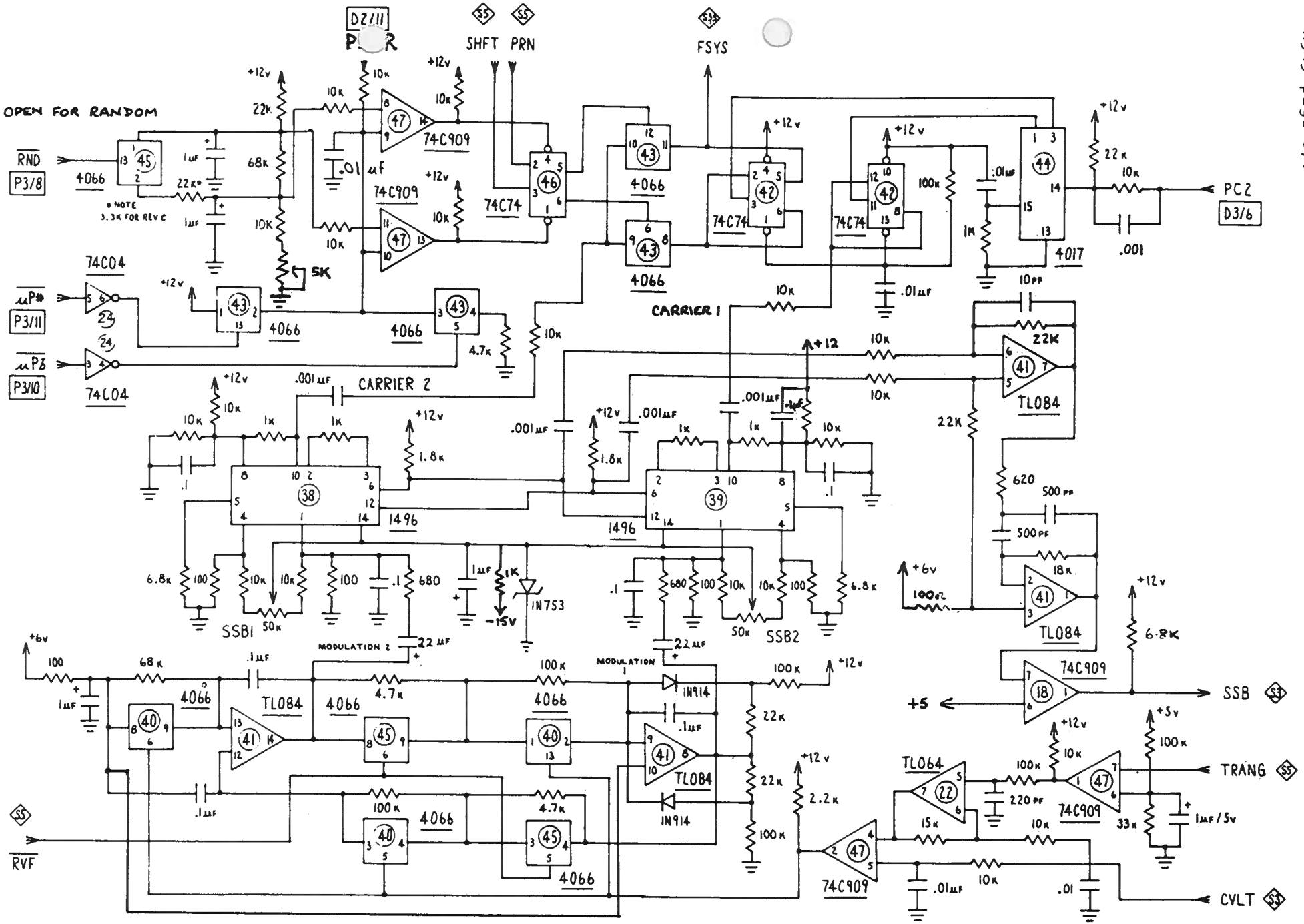


VOLTAGE CONTROLLED OSCILLATOR
AND READ FIFO CLOCK SELECT

HA 931 REV. C, D(2)
SHEET 3 OF 6

10/80

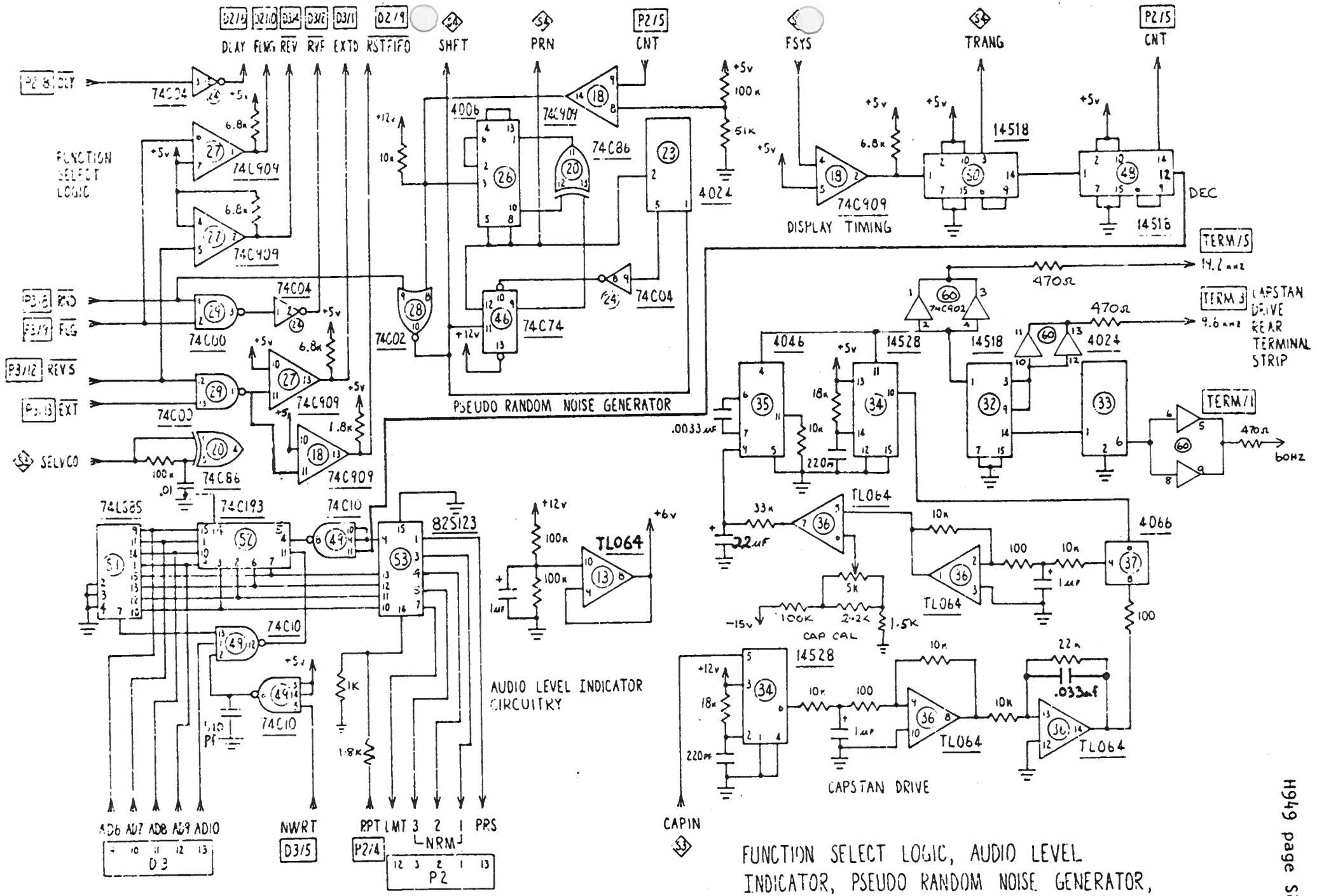
VAR 11-79



SINGLE SIDE BAND GENERATOR

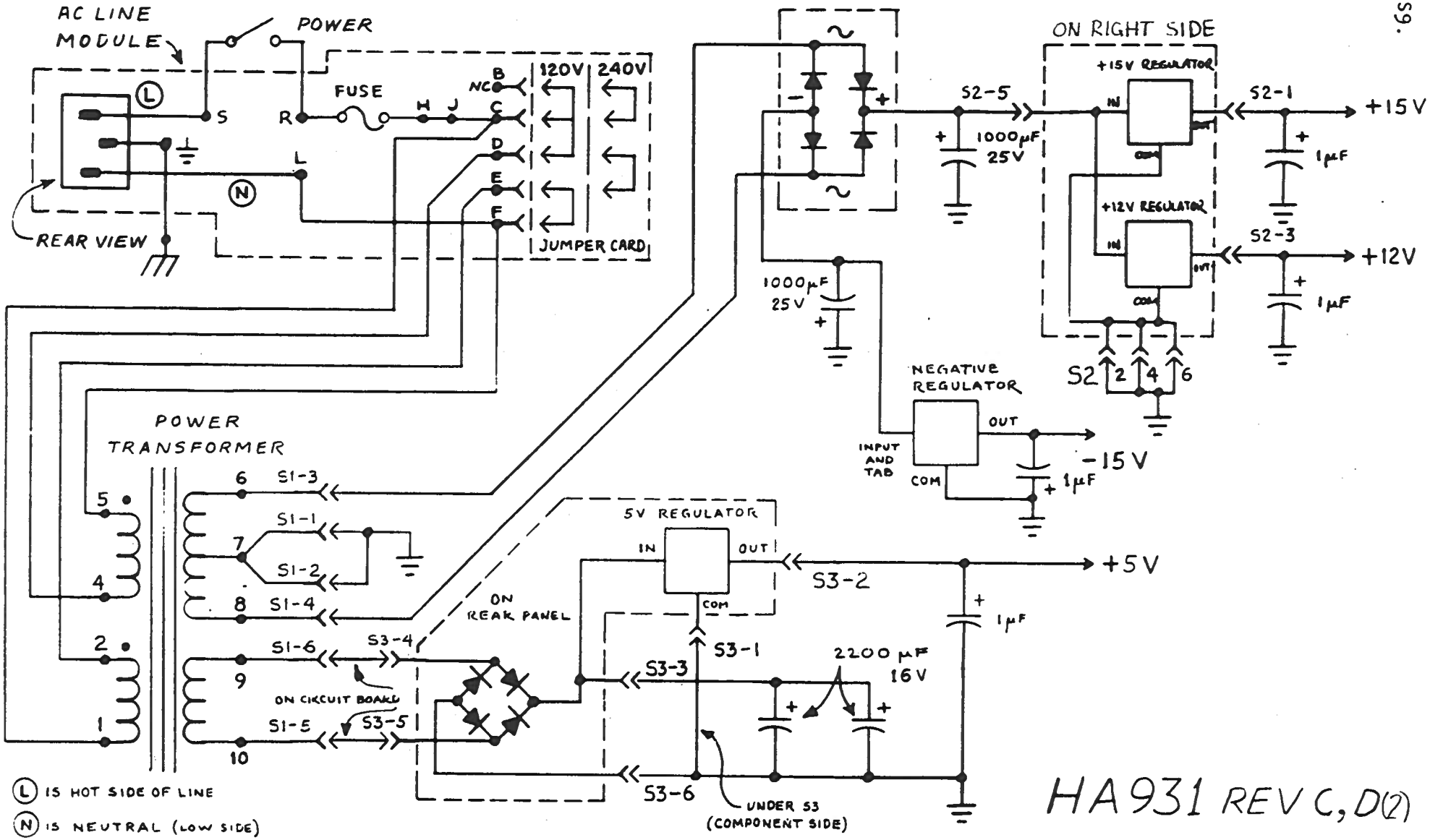
HA931 REV. C, D(2) SHEET 4 OF 6

11/82



HA 931 REV. C,D(2) SHEET 5 OF 6 11/82

FUNCTION SELECT LOGIC, AUDIO LEVEL INDICATOR, PSEUDO RANDOM NOISE GENERATOR, CAPSTAN DRIVE AND DISPLAY TIMING CIRCUITRY

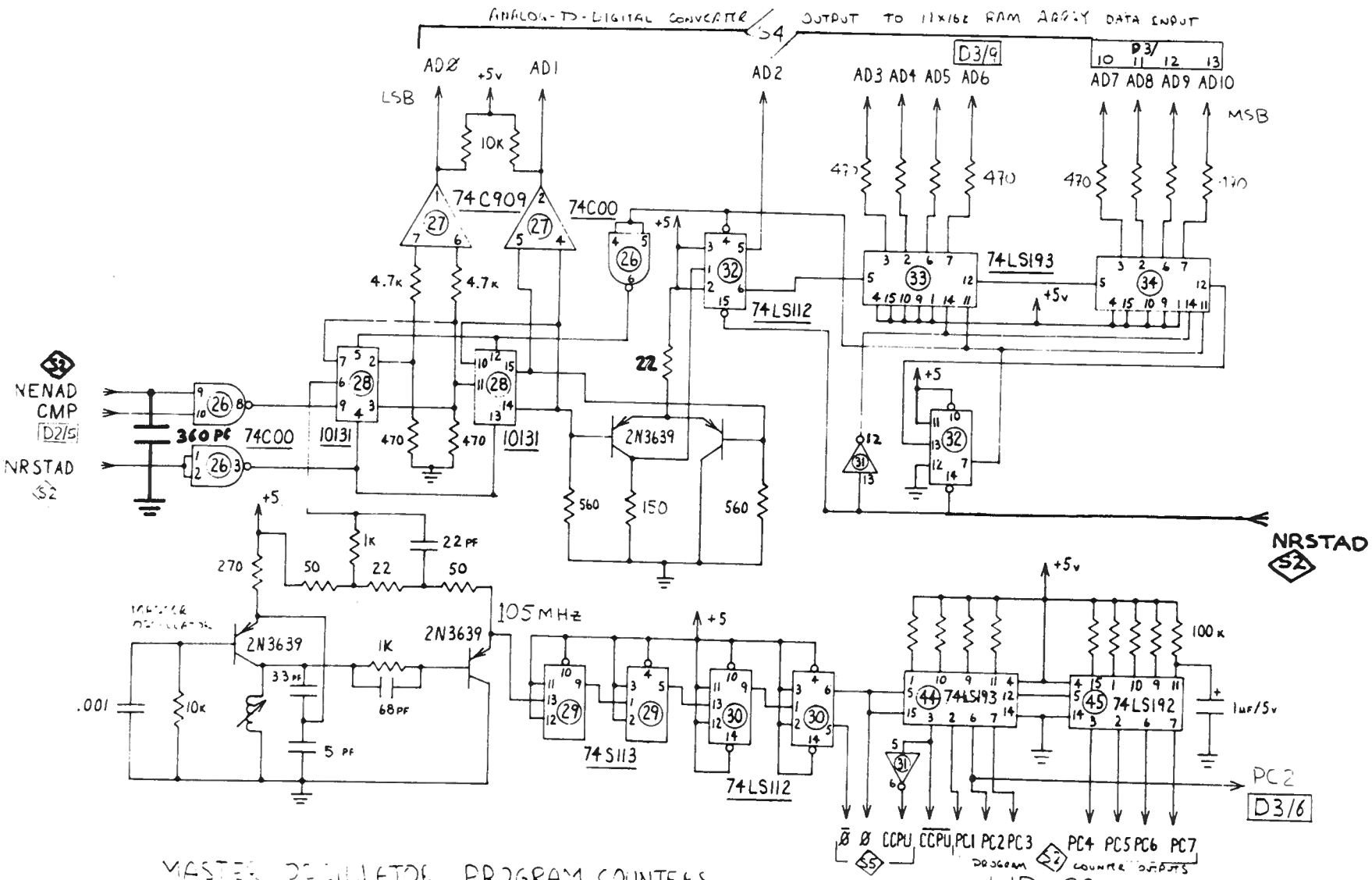


HA931 REV C, D(2)

POWER SUPPLY

SHEET 6 OF 6 10/80

AB · '679

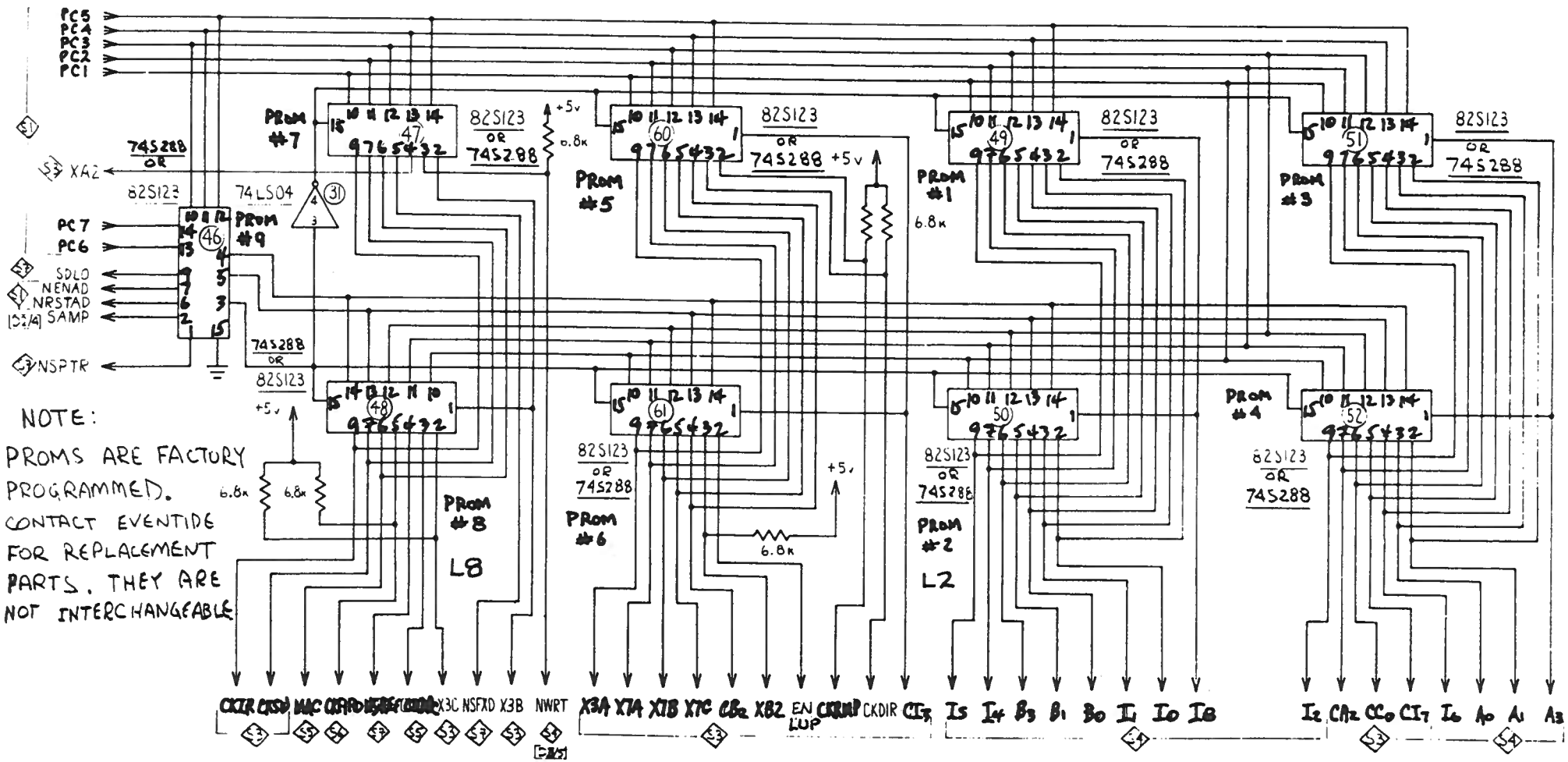


MASTER OSCILLATOR, PROGRAM COUNTERS, AND ANALOG-TO-DIGITAL CONVERTER

HD 921 REV. C. D(2)

SHEET 1 OF 7

6/84

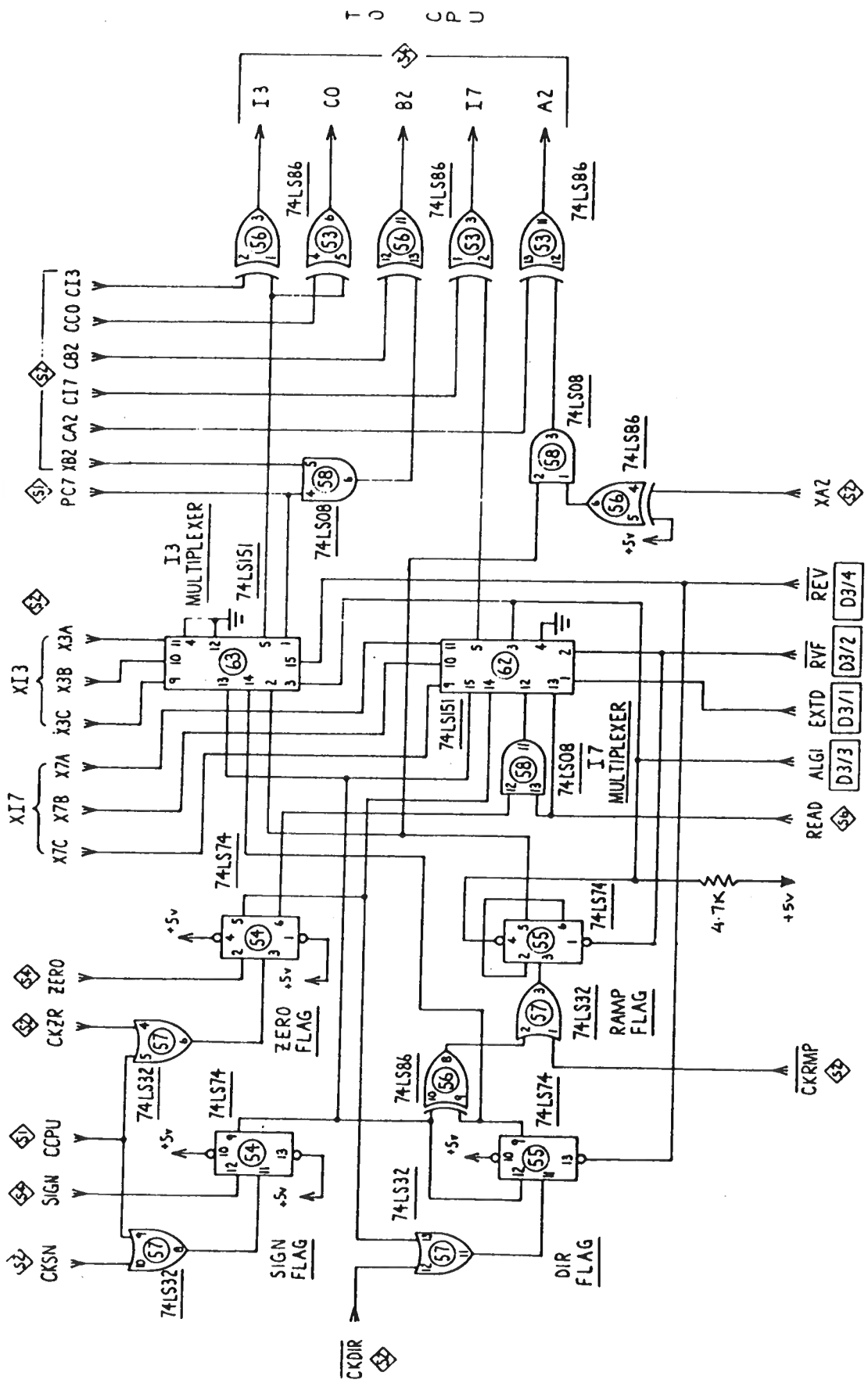


NOTE:
PROMS ARE FACTORY PROGRAMMED. CONTACT EVENTIDE FOR REPLACEMENT PARTS. THEY ARE NOT INTERCHANGEABLE

TIMING AND MICRO-INSTRUCTION
PROGRAMMABLE READ-ONLY-MEMORIES (PROMS)

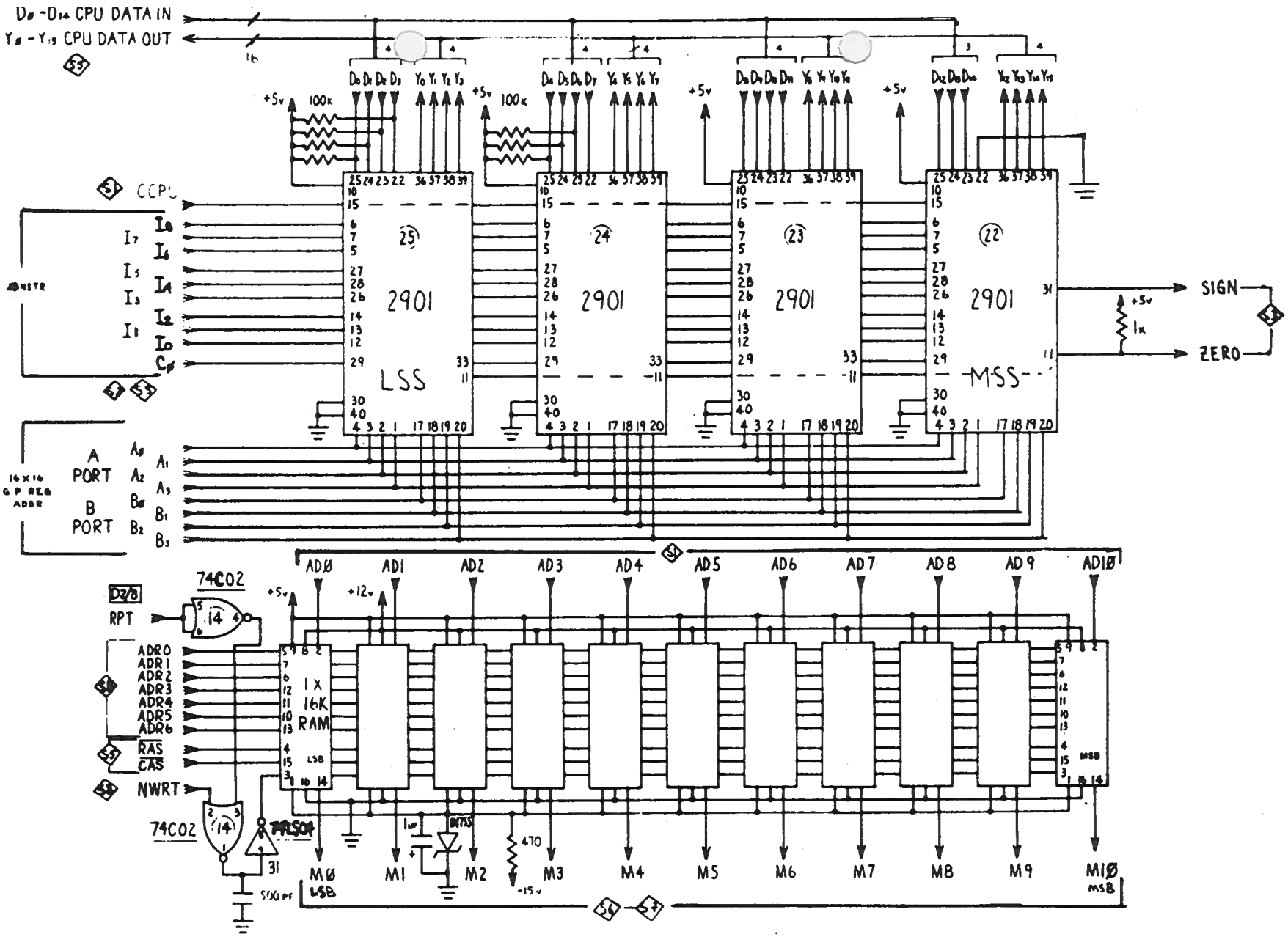
HD 921 REV. D(2)
SHEET 2 OF 7

11/82



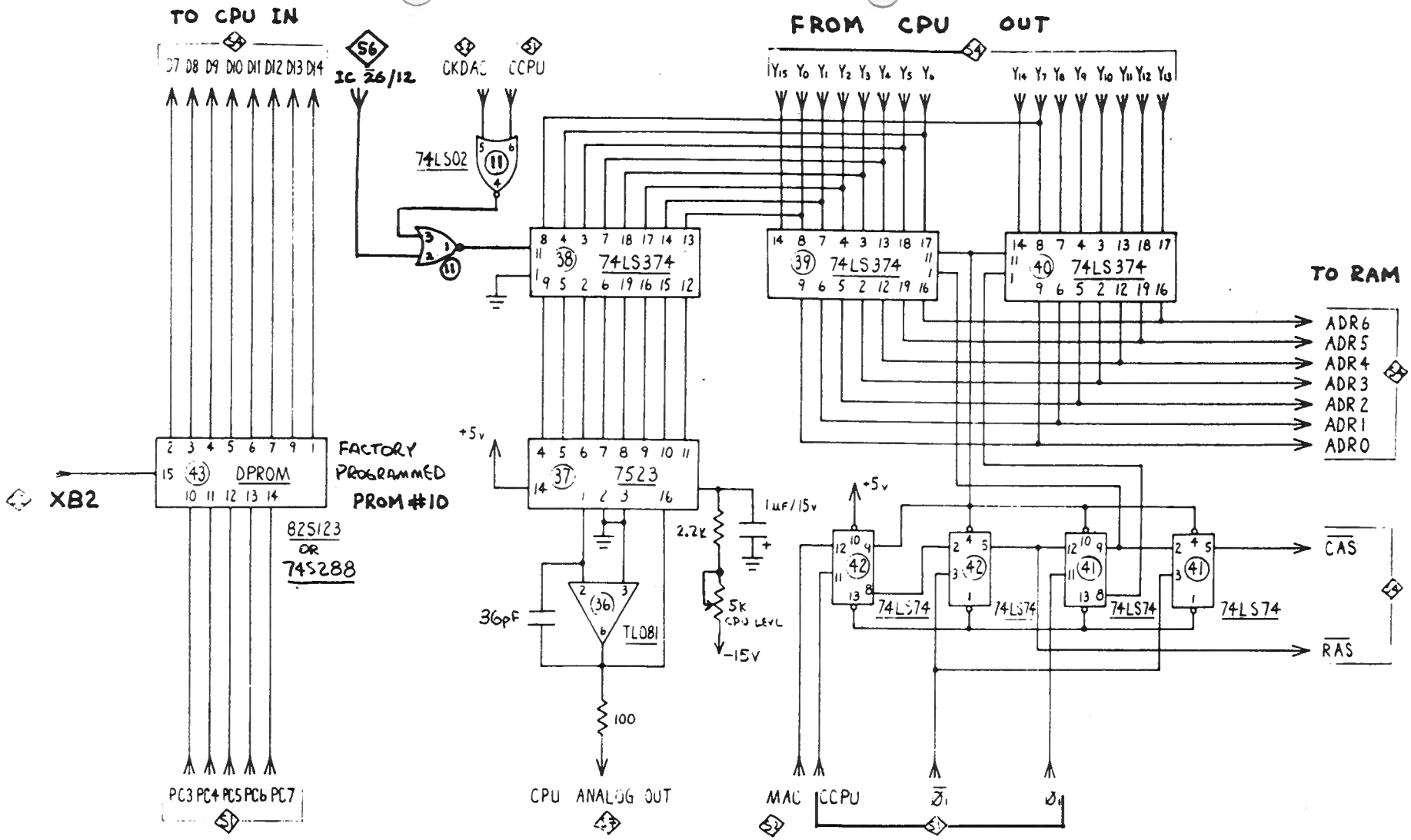
HD 921 REV. D(2)
SHEET 3 OF 7 10/80

CPU STATUS FLAGS AND
CONDITIONAL μINSTR LOGIC



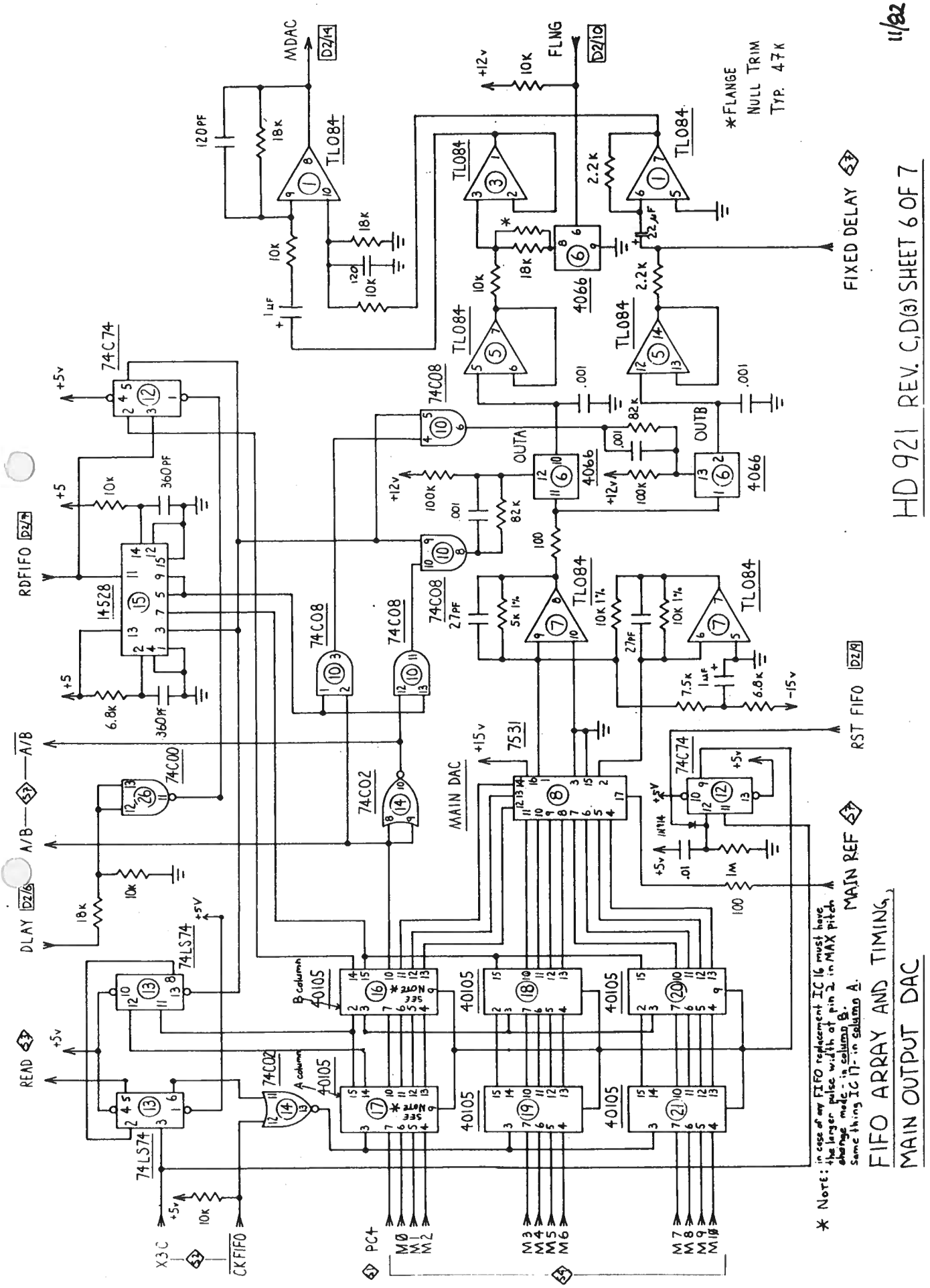
16-BIT CENTRAL PROCESSING UNIT (CPU) AND
11 x 16K DYNAMIC RANDOM ACCESS MEMORY ARRAY (RAM)

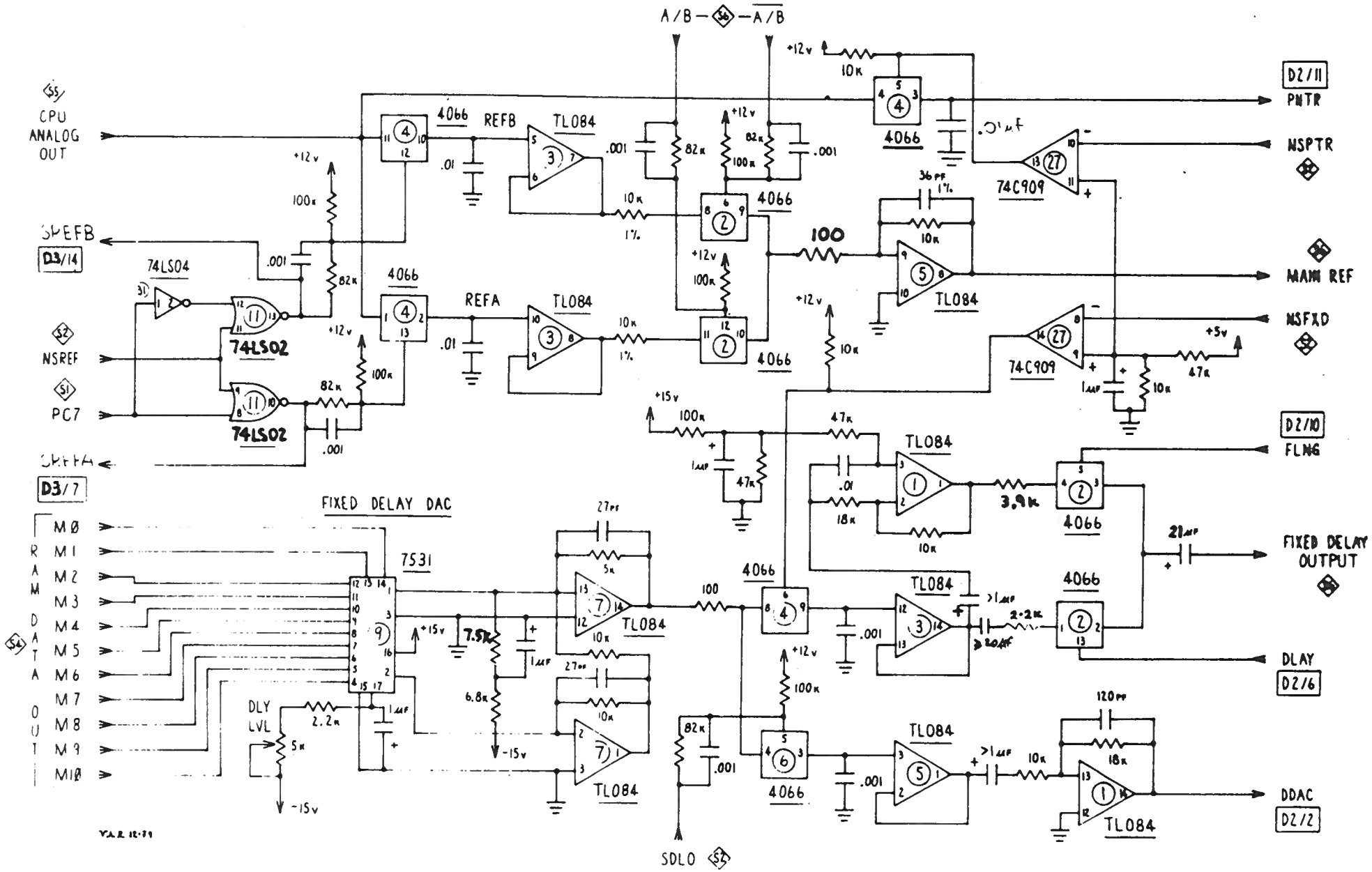
HD 921 REV. C, D(2)
SHEET 4 OF 7 10/80



DATA PROM, CPU ANALOG OUT
AND RAM ADDRESS AND TIMING

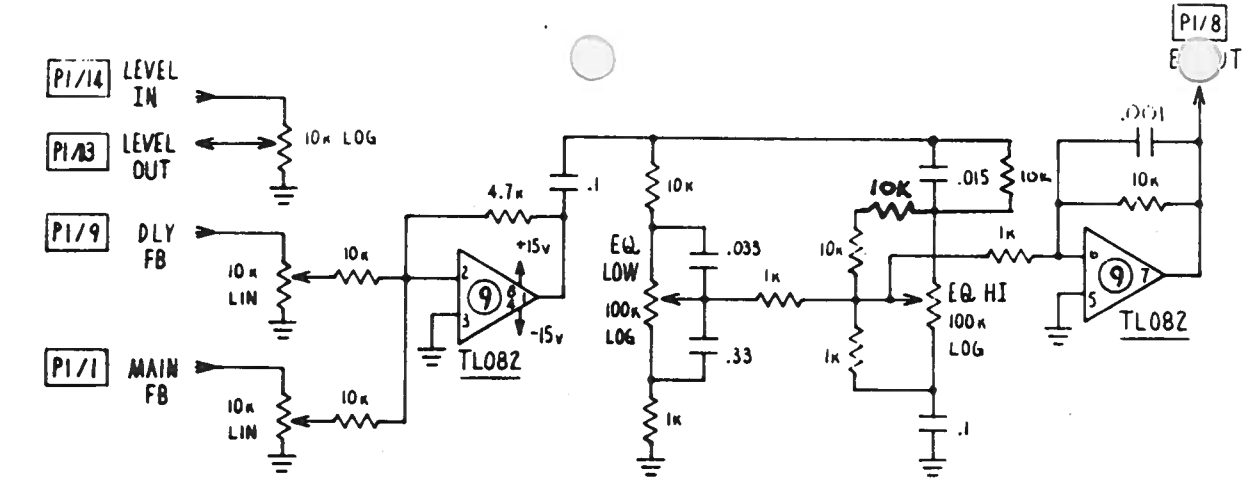
HD 921 REV. C, D(2)
SHEET 5 OF 7 11/82

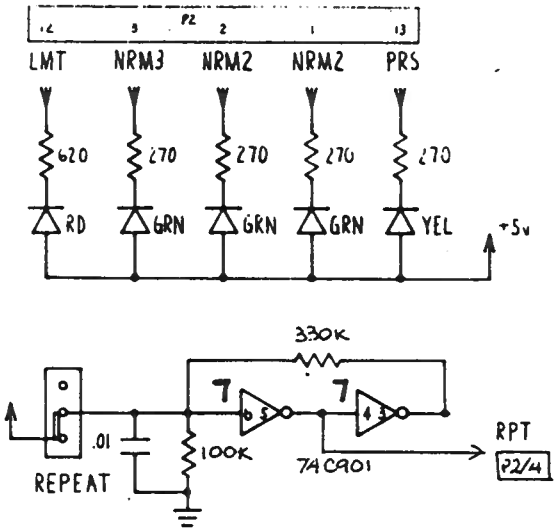

HD 921 REV. C,D(3) SHEET 6 OF 7
11/82
FIFO ARRAY AND TIMING
MAIN OUTPUT DAC
* Note: in case of any FIFO replacement IC 16 must have the larger pulse width of pin 2 in MAX pitch change mode: in column B. Same thing IC 17: in column A.
MDAC
FLNG
*FLANGE NULL TRIM TYP. 47K
FIXED DELAY
MAIN REF
RST FIFO
RDFIFO
DLAY
A/B
READ
X3C
CK FIFO
PC4
MAIN DAC
OUTA
OUTB
TL084
74C74
74C08
74C00
74C02
74LS74
14528
4066
7531
40105
M0 M1 M2 M3 M4 M5 M6 M7 M8 M9 M10

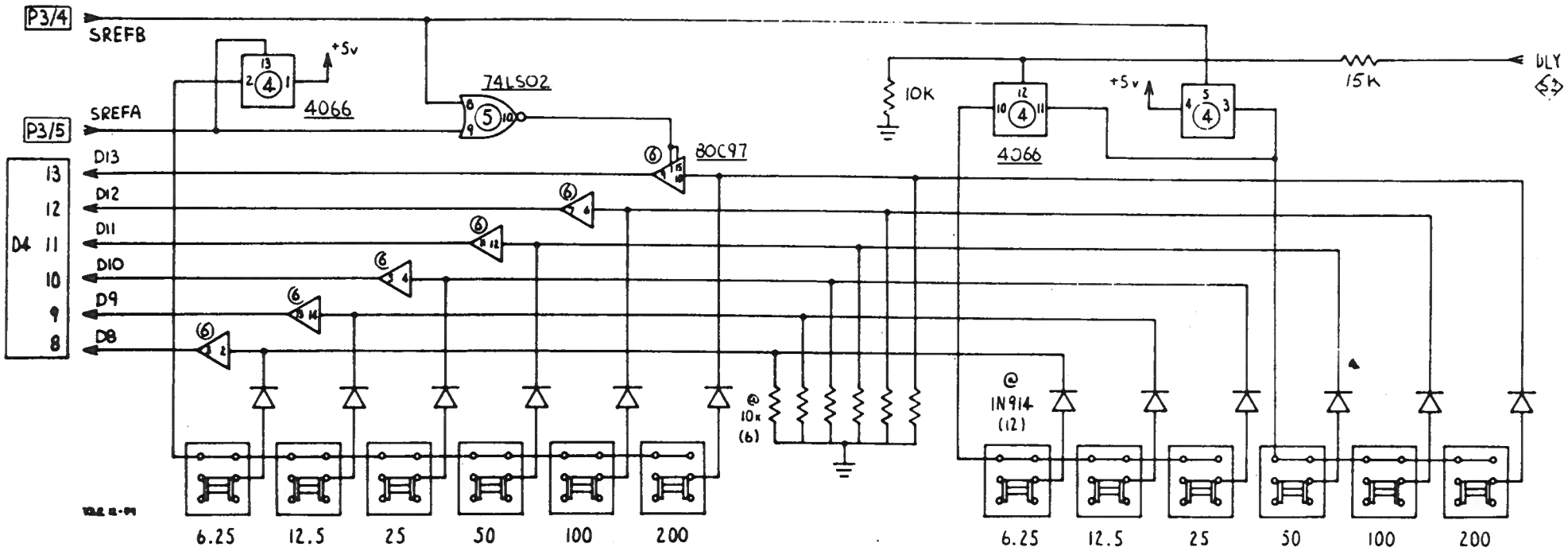


MAIN OUTPUT REFERENCE VOLTAGE
AND DELAY ONLY DAC

HD 921 REV. C,D(2)
SHEET 7 OF 7 10/80

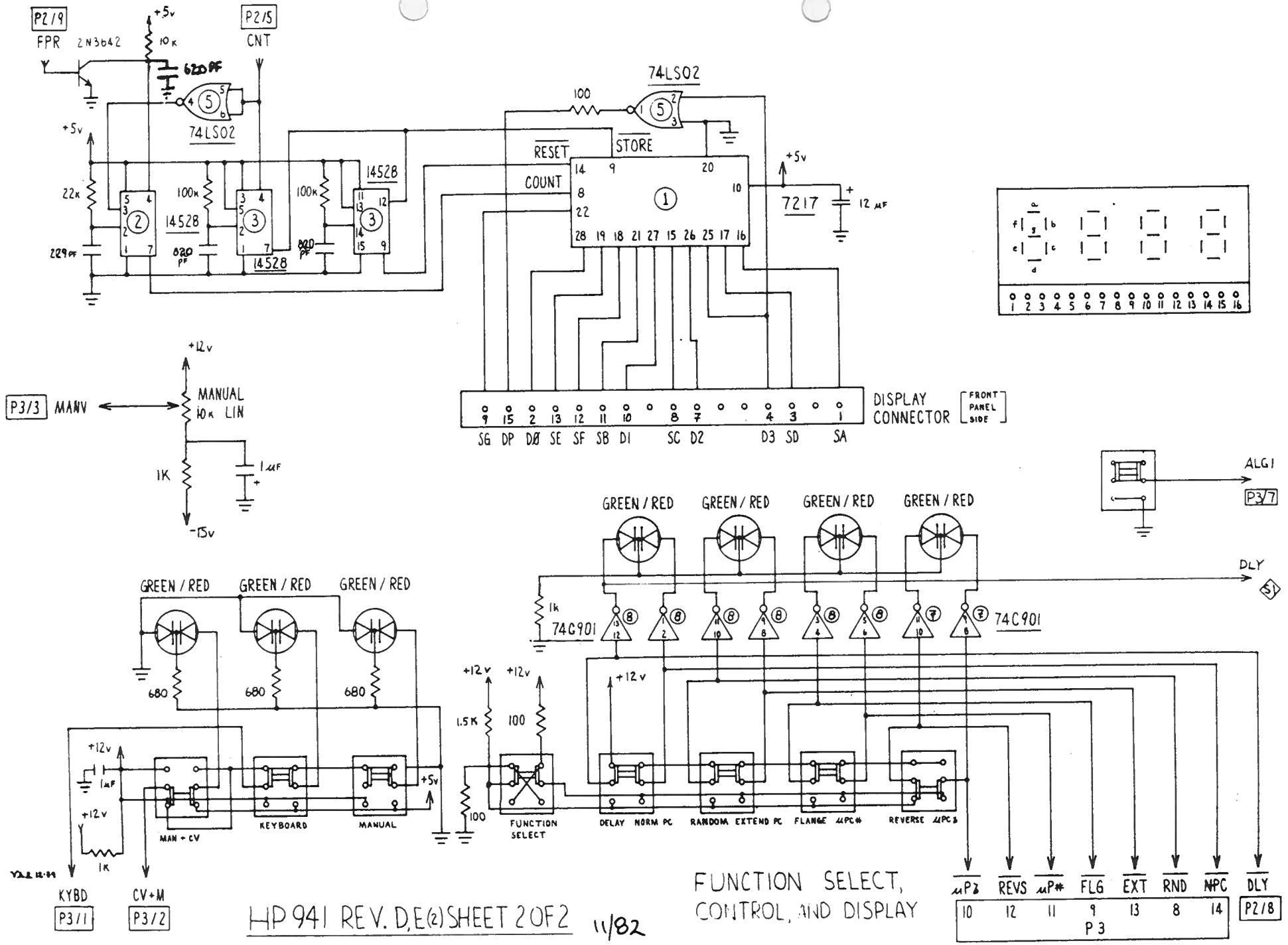






HP 941 REV. D,E SHEET 1 OF 2 10/80

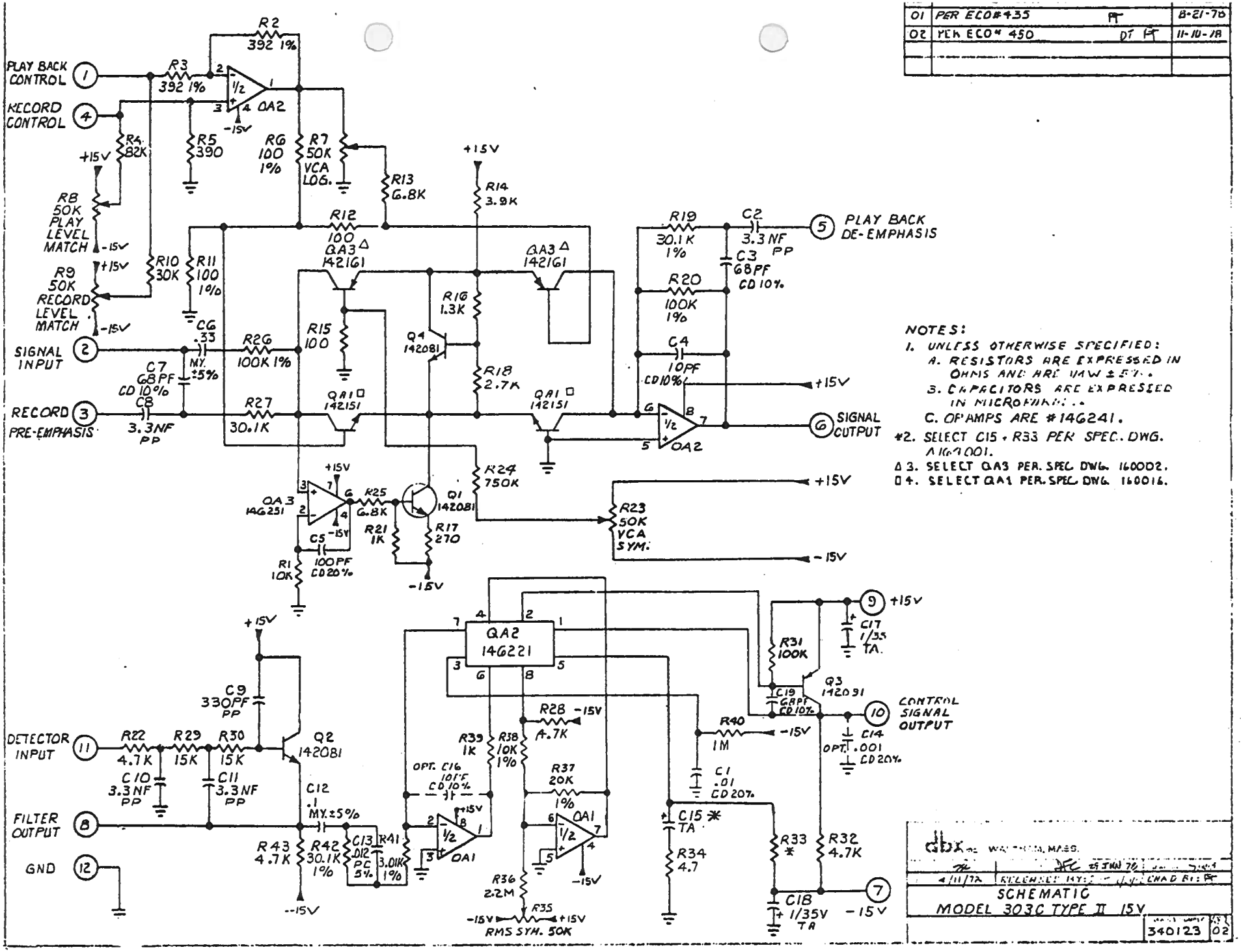
AUDIO CONTROL AND DELAY SET



HP 941 REV. D,E(2) SHEET 2 OF 2 11/82

FUNCTION SELECT, CONTROL, AND DISPLAY

01	PER ECO#435	PT	8-21-70
02	PER ECO# 450	DT PT	11-10-71



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE EXPRESSED IN OHMS AND ARE 1/4W ± 5%.
   B. CAPACITORS ARE EXPRESSED IN MICROFARADS.
   C. OP AMPS ARE #146241.
#2. SELECT C15 & R33 PER SPEC. DWG. A164001.
Δ 3. SELECT QA3 PER SPEC. DWG. 160002.
□ 4. SELECT QA1 PER SPEC. DWG. 160016.

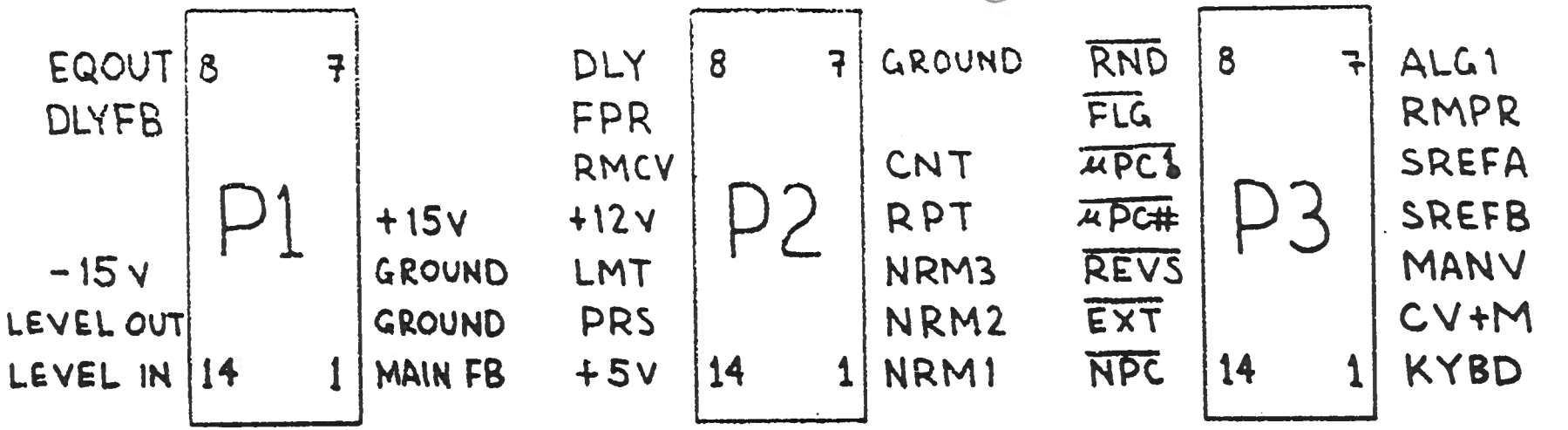
dbx inc. WALTHAM, MASS.

		25 JAN 72	
4/11/72	RELEASED BY:		DRAWN BY: PT

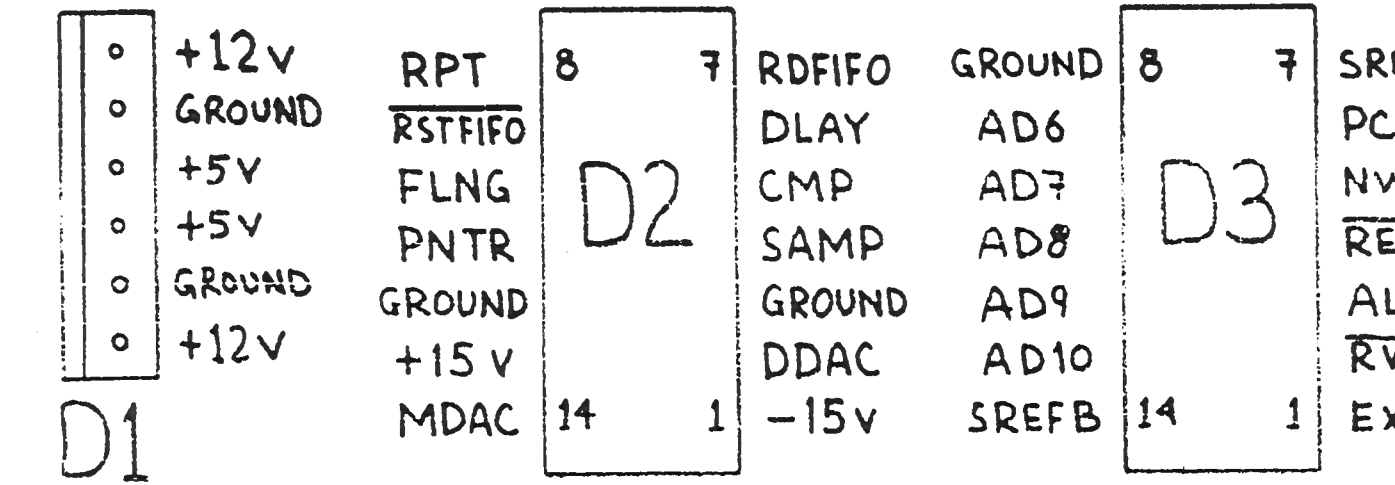
SCHEMATIC
MODEL 303C TYPE II 15V

340123 02

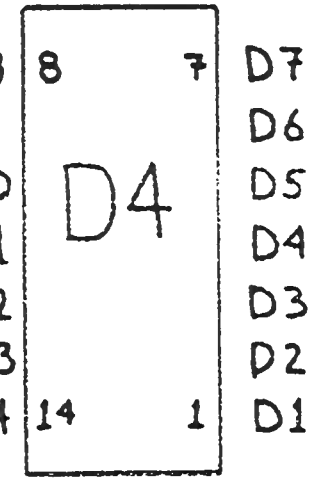
HA931 — HP941



HD921 — HA931

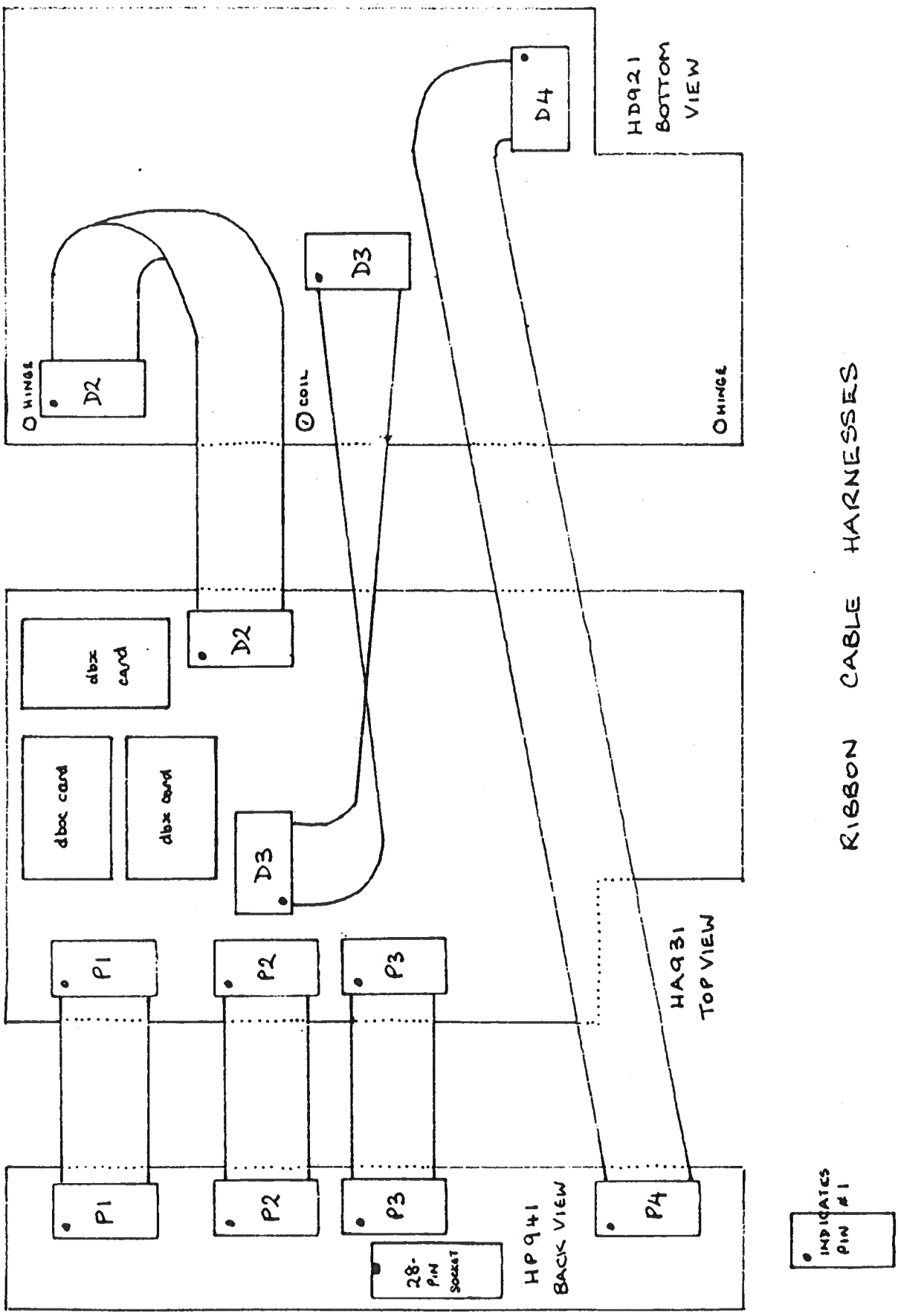


HD921-HP941



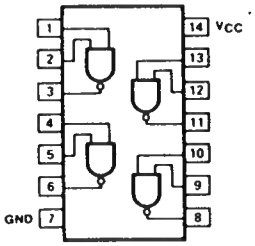
INTER-BOARD CONNECTORS

APPENDIX - Ribbon Cable Harnesses used in H949 Harmonizer

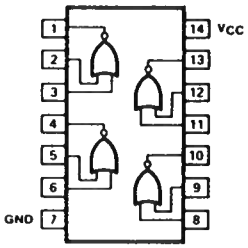


APPENDIX Integrated circuits used in H949 Harmonizer

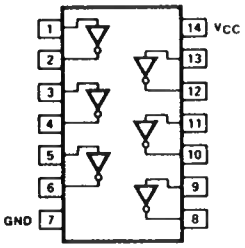
74LS00, 74C00
Quad 2-input
NAND gate



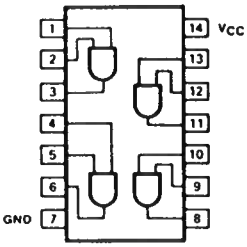
74LS02, 74C02
Quad 2-input
NOR gate



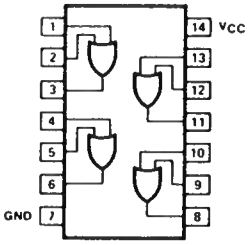
74LS04, 74C04
Hex inverter



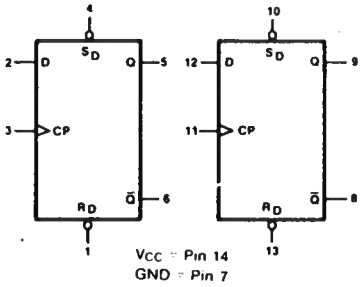
74LS08, 74C08
Quad 2-input
AND gate



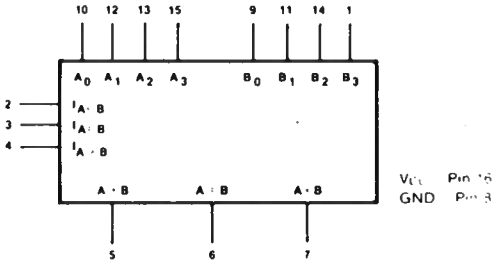
74LS32
Quad 2-input
OR gate



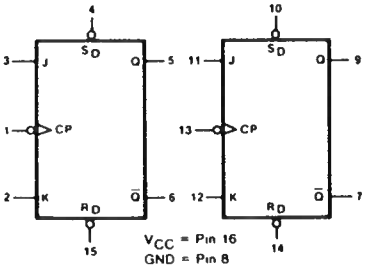
74LS74, 74C74
Dual positive edge-
triggered flip-flop



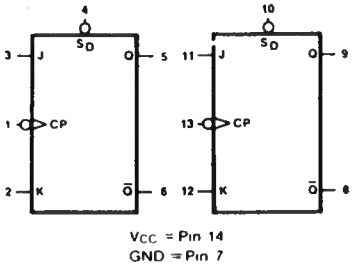
74LS85
4-bit magnitude
comparator



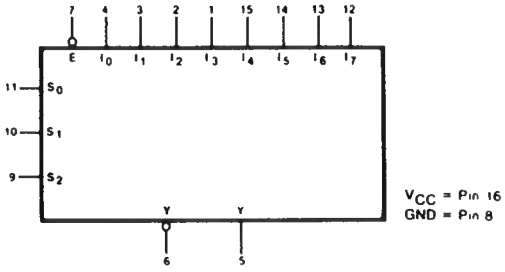
74LS112, 74S112
Dual JK negative edge-
triggered flip-flop



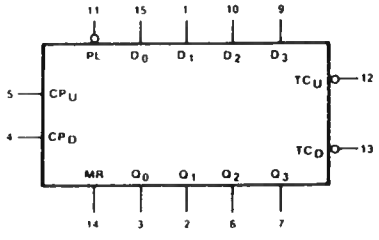
74LS113, 74S113
Dual JK negative edge-
triggered flip-flop



74LS151
8-to-1 multiplexer

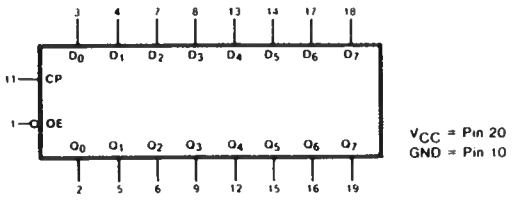


74LS192
BCD decade
up/down counter



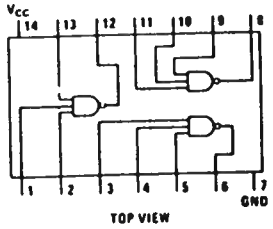
74LS193, 74C193
4-bit binary
up/down counter

74LS374
Octal D flip-flop (3-state)

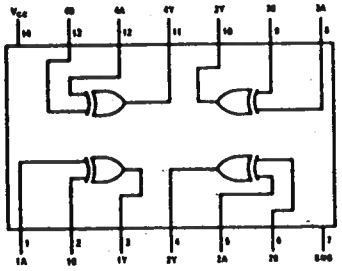


APPENDIX Integrated Circuits used in the H949 Harmonizer

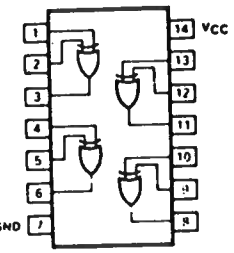
74C10
Triple 3-input
NAND gate



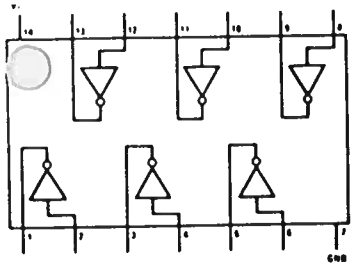
74C86
Quad 2-input
Exclusive-OR gate



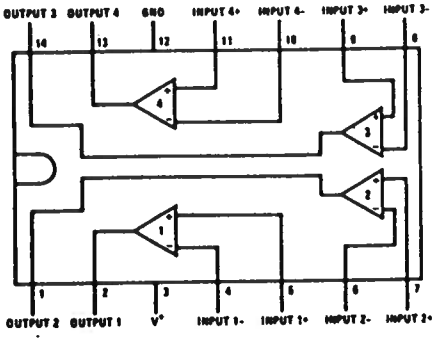
74LS86
Quad 2-input
Exclusive-OR gate



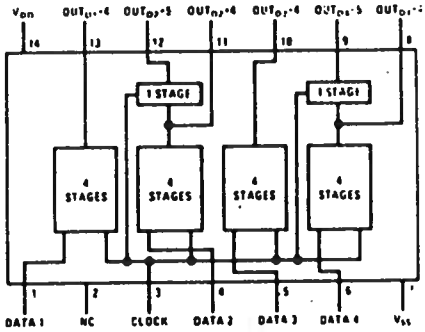
74C901
Hex inverting
TTL buffer



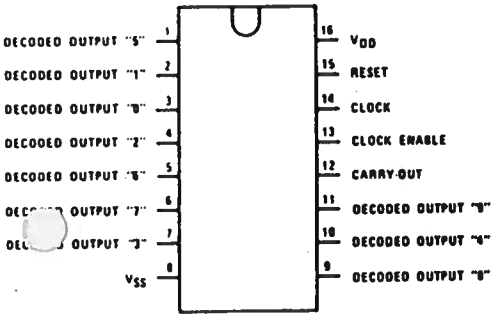
74C909
Quad comparator



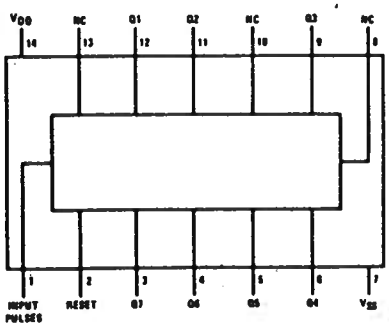
CD4006
18-stage static
shift register



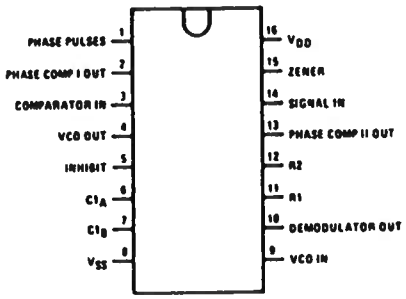
CD4017
Decade counter/divider with
10 decoded outputs



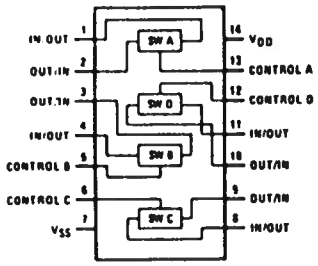
CD4024
7-stage ripple-carry
binary counter/divider



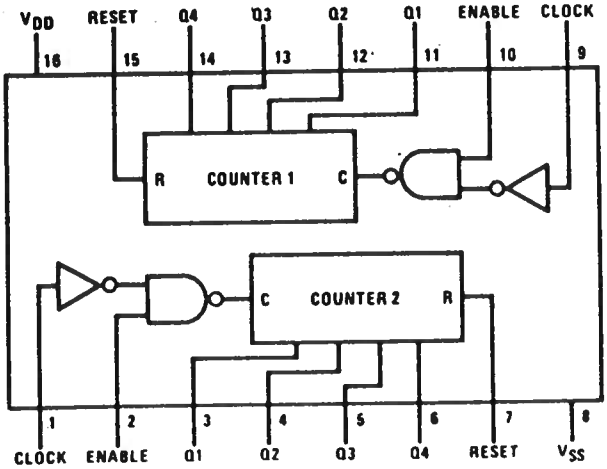
CD4046
Micropower
phase-locked loop



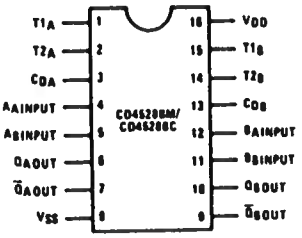
CD4066
Quad bilateral switch



CD4518, MC14518
Dual synchronous up counter

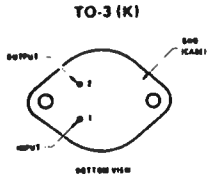


CD4528, MC14528
Dual monostable
multivibrator

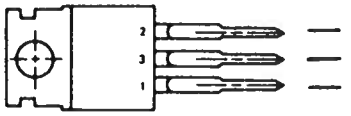


APPENDIX Integrated Circuits used in the H949 Harmonizer

LM323 - 3 amp, 5 volt positive regulator



7812UC - 12 volt regulator
7815UC - 15 volt regulator
7915UC - minus 15 volt regulator



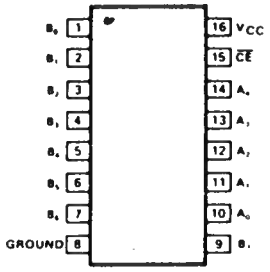
	7812UC + 7815UC	7915UC
2	output	output
3	common	input
1	input	common

82S123 or 74S288 - 256 Bipolar PROM (32 x 8)

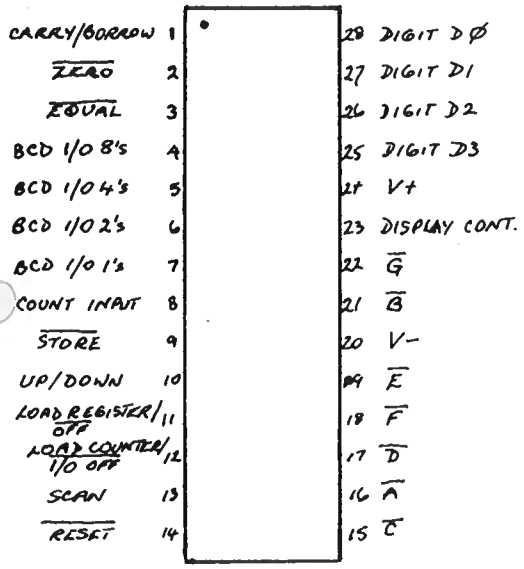
VERY IMPORTANT NOTE:

All parts with the above marking are FACTORY PROGRAMMED, and will fit only into their own specific locations on each circuit board. THEY ARE NOT INTERCHANGEABLE. For example, you cannot exchange IC60 and IC61 on the HD921 board - they have been programmed differently, and their characteristics are completely different.

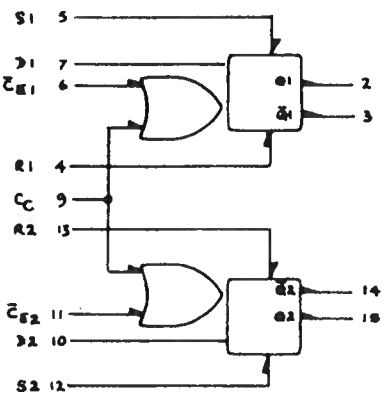
Should you ever need replacements for any of these parts, you must specify the board number and the IC number, to ensure receiving the correct replacement.



ICM7217 - Complementary MOS 4-digit Up/Down counter-decoder-driver



MC10131 Dual D-Type Master/Slave Flip-Flop



R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

CLOCKED TRUTH TABLE

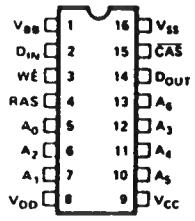
C	D	Q_{n+1}
L	Ø	Q_n
H	L	L
H	H	H

Ø = DON'T CARE
C = $\bar{C}_E + C_C$
A clock H is a clock transition from a low to a high state.

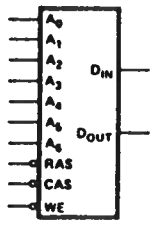
APPENDIX Integrated Circuits used in the H949 Harmonizer

16 K Dynamic RAM (various manufacturers and part numbers)

PIN CONFIGURATION



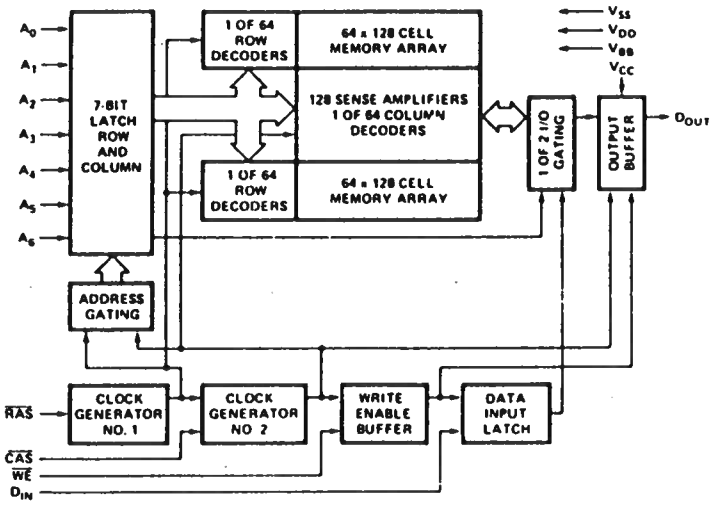
LOGIC SYMBOL



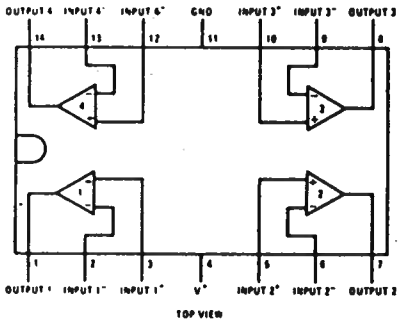
PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

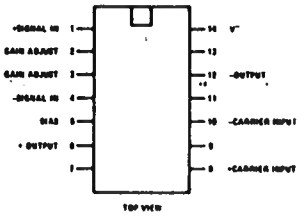
BLOCK DIAGRAM



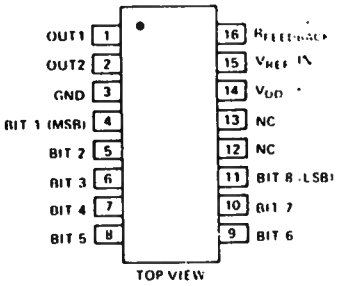
TL064
Quad op amp



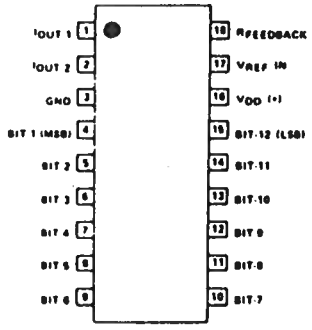
LM1496
Balanced modulator-demodulator



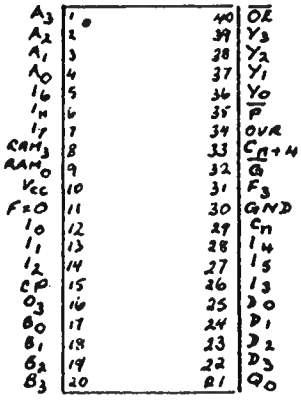
AD7523
8 Bit D/A converter



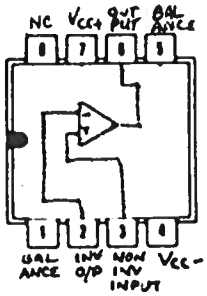
AD7531 - 4-Quadrant Multiplying D/A Converter



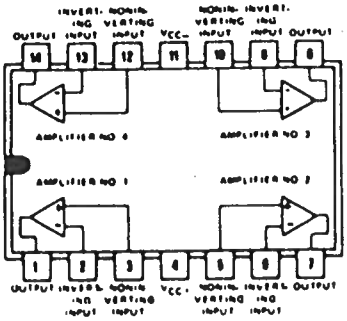
AM2901 - Four-bit bipolar micro-processor slice



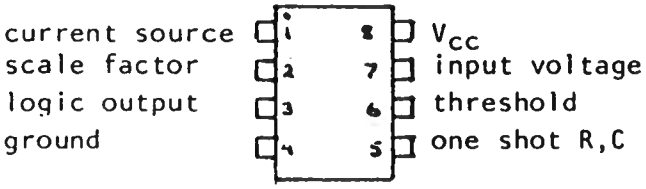
TL081 - JFET-Input Operational Amplifier



TL084 - JFET-Input Quad Operational Amplifier



RC4151 - Voltage to Frequency Converter



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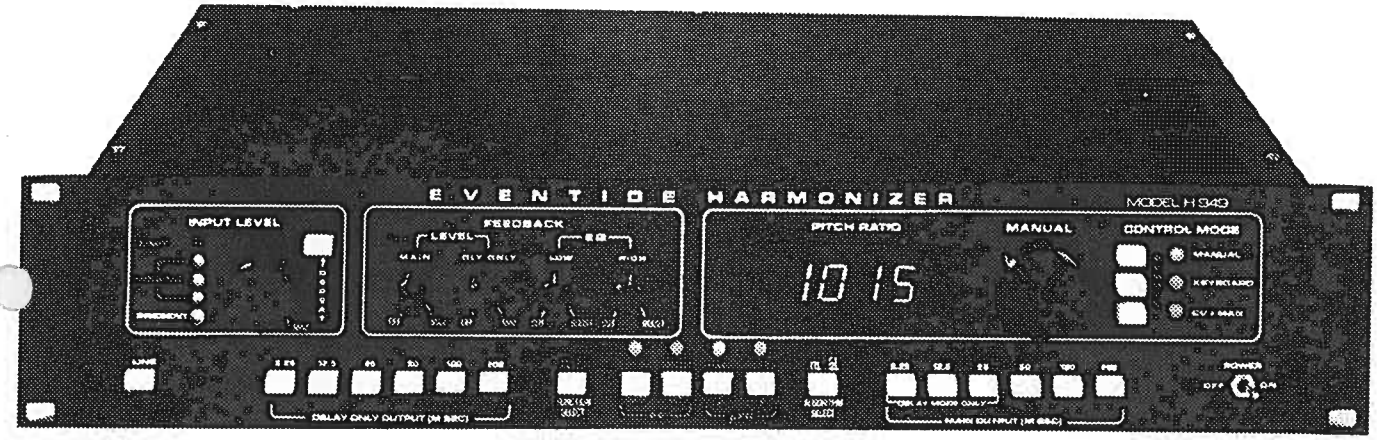
MODEL H949 HARMONIZER®



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