6809 TEST CONSOLE

TEST PROGRAM

OPERATING INSTRUCTIONS

Strand Lighting

6809 TEST CONSOLE, TEST PROGRAM OPERATING INSTRUCTIONS

CONTENTS

	PAGE NO
INTRODUCTION	1
TVDU - V.D.U. TEST	2
CPTST3 - CHANNEL PROCESSOR TEST, VERSION 2	5
TCKSM - PROM CHECKSUM TEST	8
TMEM - MEMORY TEST	10
GBEXTST-A1 - GALAXY BACK-UP EXECUTIVE TEST	17
GBCPTST-A1 - GALAXY BACK-UP CHANNEL PROCESSOR TEST	19
FDTEST-A3 - FLOPPY DISC TEST	22
APPENDIX 1 - Discontinued Test Programs	28
APPENDIX 2 - Use of 6809 Test Programs	29

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Introduction

The set of test programs is designed to operate using the Strand Lighting 6809 Test Console. For most tests a data terminal must be connected to the Test Console in order to enter commands, and read data on error conditions.

For operational details of Console and Terminal, see the 6809 Test Console Handbook.

The test programs were designed to prove correct operation of certain hardware functions, and as such, may be used as an aid to fault diagnosis.

No instructions are given as to the interpretation of test program error reports, as a full interpretation can only be made if other information is taken into account. The fault condition indications and other test results will be required.

Some test programs consist of several subtests. These should be run in numerical order as subsequent subtests often assume that the previous test has verified certain parts of the hardware as fully operational, and inconsistent error reports are possible if the assumption is untrue.

Appendix 2 gives some guidelines as to which tests are applicable to different sections of hardware, within Strand Lighting current products.

While every effort has been made to ensure that the information provided herein is correct, please feel free to notify us in the event of any error or inconsistency.

TVDU (V.D.U. Test)

The test program is stored in a PROM which uses a start address of $E800.

The tests are used to check V.D.U.'s and V.D.U. interface cards. Each test displays patterns of characters on V.D.U. screens.

Tests

A. Start address $E800
Fills screen of each V.D.U. with the V.D.U. number.

B. Start address $E803
Fills screen, of the selected V.D.U., with each ASCII character in turn.

C. Start address $E806
Displays, on the selected V.D.U., characters using all monochrome attributes.

D. Start address $E809
Displays, on the selected V.D.U., characters using all colour attributes.

E. Start address $E80C
Fills a V.D.U. screen with a character as selected from the test console switches.

F. Start address $E80F
Sends a crosshatch pattern to the selected V.D.U.

To run the tests:-

1. Set up the Test Console with the TVDU PROM in the I.C.2 slot of the test PROM card.

2. Reset the system in 'console' mode i.e. Restart Console.

To run tests with a terminal connected to the test console.

1. Each test is started by typing 'S' followed by the start address of the test, followed by 'CR'

2. Tests A and E then run with no further terminal entries.

3. Tests B, C, D, and F send question 'V.D.U. NO?' to the terminal. The required V.D.U. number should be entered, followed by 'CR' . The test will then run and requires no further terminal entries.

To run tests without a terminal

1. For tests A and E, enter the start address on the keypad, press LOAD ADDRESS, press START.

   The test will then run.

2. For tests B, C, D, and F, the V.D.U. number must first be set up as a binary count on Test Console switches SW15, SW14. The test is then started as in step 1.

For test E, data is entered via the Test Console Switches to control the character, attribute, and V.D.U. number. The use of each switch bit is given in the list below.

Test Console Switch Positions.

SW15) V.D.U number
SW14)

SW13)
SW12)
SW11) Colour Attribute
SW10)

SW9) Monochrome Attribute
SW8)

SW7) Not Used
SW6)

SW5)
SW4)
SW3) Character Code
SW2)
SW1)
SW0)

Character Code

This is the reduced 64 character ASCII upper case set, presented on D0-D5. (D6,7 not used)

				0	0	1	1	=D5
				0	1	0	1	=D4
D3	D2	D1	D0					
0	0	0	0	@	P	space	0	
0	0	0	1	A	Q	!	1	
0	0	1	0	B	R	"	2	
0	0	1	1	C	S	#	3	
0	1	0	0	D	T	$	4	
0	1	0	1	E	U	%	5	
0	1	1	0	F	V	&	6	
0	1	1	1	G	W	'	7	
1	0	0	0	H	X	(	8	
1	0	0	1	I	Y	)	9	
1	0	1	0	J	Z	*	:	
1	0	1	1	K	[	+	;	
1	1	0	0	L	\	,	<	
1	1	0	1	M	]	-	=	
1	1	1	0	N	^	.	>	
1	1	1	1	O	_	/	?	

TVDU can check up to 4 V.D.U's, i.e. 2 Ref 1702 Cards. Each V.D.U. being uniquely selected by the Attribute register. The Attribute register is also used to define the character attribute for the V.D.U. character written directly into the V.D.U. memory map. This memory is WRITE ONLY.

ATTRIBUTE REGISTER

D7	0	0	1	1
D6	0	1	0	1
VDU No	0	1	2	3

D5)
D4) COLOUR CODE
D3) 0 - F
D2)

D1) MONOCHROME ATTRIBUTES
D0) 0 - 3

0 Normal character
1 Flashing character
2 Inverse video
3 Dim character

COLOUR CODE

Code	Char	Background	
0	R	-	RED/BLACK
1	G	-	GREEN/BLACK
2	-	B	BLACK/BLUE
3	RG	-	YELLOW/BLACK
4	RB	-	MAGENTA/BLACK
5	GB	-	CYAN/BLACK
6	RGB	-	WHITE/BLACK
7	RG	R	YELLOW/RED
8	-	R	BLACK/RED
9	-	G	BLACK/GREEN
A	B	RB	BLUE/MAGENTA
B	GB	B	CYAN/BLUE
C	R	RG	RED/YELLOW
D	-	RG	BLACK/YELLOW
E	-	GB	BLACK/CYAN
F	B	GB	BLUE/CYAN

CPTST 3 (Channel Processor Test)

The test program is stored in a PROM which uses a start address of $E800.

The test will check channel processors in any slots of a system.

A terminal must be connected to the terminal input of the Test Console in order to operate the test.

The test consists of four subtests:-

Test 0 - C.P. Selection.

(This test performs checks on the Executive access circuitry on each channel processor).

The R.A.M. of all C.P's under test is cleared and checked for illegal bits.

The R.A.M. of all C.P's has every bit set and then individually checked.

Then, leaving the background pattern as $FF, each C.P. is accessed individually and has an ascending count written into its R.A.M. After writing the pattern into each C.P., the contents of R.A.M. on each C.P. is checked for errors.

Test 1 - Static Pattern

This test performs a simple check on Channel Processor R.A.M, and its ability to hold data over a period of time.

The R.A.M. of each C.P. is written with a data pattern. The data is then repetitively read and checked, without being re-written.

Test 2 - Sliding Read/Writes

This test performs a more complex check on Channel Processor R.A.M.

The R.A.M. of each C.P. is written with a data pattern. The data is then read and checked.

On subsequent passes the data pattern is shifted by one memory location.

Test 3 - C.P. Program

This test checks the ability of Channel Processors to run a simple program.

The Executive writes a program into the 'top' of C.P. R.A.M. and then sets it to run. The program writes an ascending count to the lowest 256 bytes of C.P. R.A.M. and then stops.

The Executive then checks the data pattern.

The test is then repeated until each 256 byte block of C.P. R.A.M. (except the program area) has been tested.

To run the tests

1. Set up the Test Console with the CPTST3 PROM in the I.C. 2 slot of the test PROM card.

2. Set Test Console switches as appropriate:

SW.15	up	Halt on error. (once halted, the test can be resumed by setting SW. 15 down).
SW.14	up	Suppress 'end of pass' messages.

3. Reset the system in 'console mode' i.e. Restart Console.

4. Press 'START' - the test program will start from the Test Console start vector.

The message

FIRST CP? (O-F)

is output.

Enter a hexadecimal number indicating the lowest numbered channel processor to be tested, followed by 'CR' .

The message

LAST CP? (O-F)

is output.

Enter a hexadecimal number indicating the highest numbered channel processor to be tested, followed by 'CR' .

n.b. Channel Processors to be tested must be in a continuous group.

The message

TEST NO? (0-3)

is output.

Enter the number of the required test followed by 'CR' .

If an illegal digit is entered for any question, the question message will be re-output.

The test will then start to run.

Each test will output a 'heading':

Test 0 - TEST 0 - CP SELECTION
Test 1 - TEST 1 - STATIC PATTERN
Test 2 - TEST 2 - SLIDING READ/WRITES
Test 3 - TEST 3 - CP PROGRAM

As each test completes, it re-runs until a system reset is actioned.

If Test Console Switch 14 is down, 'end of pass' messages will be output.

The program outputs a message at the end of the first pass, and then only after each tenth pass.

If errors are detected, the test program will output error messages. These messages will normally indicate that the data read from locations in C.P. R.A.M. was not what was expected.

Error message format:-

CP-WR	CP-RD	CP-ADDR	GOOD DATA	BAD DATA
02	02	001E	FF	FE
02	02	001F	FF	FE

CP-WR = Number of Channel Processor into which data was written.

CP-RD = Number of Channel Processor from which data was read.

These two values will normally be the same, except in Test 0, where CP-WR 10 indicates a simultaneous write to all Channel Processors.

CP-ADDR Address of failed R.A.M. location. The address is given with respect to the Channel Processor address map.
i.e. R.A.M. addresses $0000 to $OFFF.

GOOD DATA The data which was originally written into the R.A.M.

BAD DATA The data which was read from the R.A.M.

For Test 3 a different error message is possible:

CP TIMEOUT Followed by number of failed C.P.

This indicates that the Executive did not detect that the Channel Processor had completed its program routines within the allocated time.

TCKSM (PROM Checksum Test)

A checksum is the result of successively adding together each location within a memory device. The technique can be used for checking program PROMs as any bit failure gives an incorect checksum.

The test program is stored in a PROM which uses a start address of $E800.

Because of the Test Console address overlay, the test will not check any PROM with addresses in the range $E000 to $FFFF. Attempting to check at such addresses either results in an error (flashing address and data displays on the console) or an incorrect checksum.
PROMs which normally reside in addresses $E000 to $FFFF should be 'moved' to another location. n.b. Observe normal precautions for handling static sensitive devices when unplugging and replugging PROMs.

To run the test

1. Set up the Test Console with the TCKSM PROM in the I.C.2 slot of the test PROM card.

2. Reset the system in 'console' mode, i.e. Restart Console.

3. Press 'Start' - the test program will start from the Test Console start vector.

4. Set Test Console switches 0 - 15 to indicate the start address and page number of the PROM under test.

Switches 0 - 7 (PROM start address)

The table below gives switch settings for 2716 PROMs. Larger PROMs require the use of less 'start addresses' (The start address for each PROM is written on the PROM label). The switch settings form a binary code for the two most significant digits of the PROM start address.

0 = switch down 1 = switch up

Start Addr.	SW7	SW6	SW5	SW4	SW3
$6000	0	1	1	0	0
$6800	0	1	1	0	1
$7000	0	1	1	1	0
$7800	0	1	1	1	1
$8000	1	0	0	0	0
$8800	1	0	0	0	1
$9000	1	0	0	1	0
$9800	1	0	0	1	1
$A000	1	0	1	0	0
$A800	1	0	1	0	1
$B000	1	0	1	1	0
$B800	1	0	1	1	1
$C000	1	1	0	0	0
$C800	1	1	0	0	1
$D000	1	1	0	1	0
$D800	1	1	0	1	1

$E000 - $FFFF give error condition

Switches 8 - 15 (PROM page number).

The switch settings form a binary code indicating a PROM page number (this is shown on the labels of relevant PROMs).

For unpaged PROMs the page number should be set to zero.

For paged PROMs the start address of each PROM must also be set.

The table below gives switch settings for pages O - F

Page No	SW11	SW10	SW9	SW8
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

SW 12 - 15 must be set at 0 (down)

5. Enter a number, representing the PROM size, on the console keyboard.

0 - 256 bytes
1 - 512 bytes
2 - 1K bytes
3 - 2K bytes (2716)
4 - 4K bytes (2732)
5 - 8K bytes (2764)
6 - 16K bytes (27128)
7 - 32K bytes (27256)

Keys 8 - F give error indication

The program will then run once giving an indication of the PROM start address in the Console Address display, and the two least significant digits of the resulting checksum in the Console Data display. (These two digits are sufficient to give reliable checksum testing).

To re-run the test, operate the 'NMI' switch. The PROM address and/or page number may be changed before re-running the test, thus enabling fairly rapid testing of sets of PROMs.

The expected Checksum for each PROM depends upon the program contents. The relevant list of Checksums (obtainable from Strand Lighting Engineering Service Department) should be consulted.

TMEM (Memory Test)

The test program is stored in a PROM which uses a start address of $E000.

The test contains four different R.A.M. tests, three of which consist of a number of subtests.

1. Processor R.A.M. test. Start address $E000.

   Tests 8K of memory from $0000 - $1FFF

2. Paged Memory Test. Start address $E002.

   Tests 1 - 128 pages of Cue Memory with a page size of 4K. The start address of the paged memory is $4000 with a Page Register at $5000.

3. Unpaged Memory Test. Start address $E004

   For testing memory between any specified Start Address and End Address. (inclusive)

4. Test Console Switch Data Memory Test. Start address $E006.

   This test uses a data byte read from the Test Console switches as test data. The R.A.M. start and end address are loaded prior to commencing this test.

The TMEM test is easier to run if a terminal is connected to the Test Console, although the test is usable without a terminal.

To run the tests

1. Set up the Test Console with the TMEM PROM in the I.C.1. slot of the test PROM card.

2. Reset the system in 'console mode' i.e. Restart Console.

   The running of each test is different:

1. PROCESSOR R.A.M. TEST

   Operation with Terminal.

1. Type in SE000 followed by 'CR'

   The message

   TEST NO.?

   is output.

The Test numbers are:

0	Do tests 1 - 6 in sequence.
1	Clear all bits, set all bits.
2	Count.
3	Checker board pattern.
4	Addres/Data Line Check.
5	Pattern
6	Immediate Write/Read Verify

2. Type in the number of the test required, followed by 'CR'

The test then runs.

Successful completion of a test (or tests) is indicated by the message 'END OF PASS 01', after which the test starts again. The number of successful passes is displayed on the Test Console LEDs, L0-L7, as well as in the 'END OF PASS xx' message.

Operation without Terminal

1. Set Test Console switches SW0 - SW3 with a binary count indicating the required subtest number.

2. Enter E000 on the Test Console keyboard.

3. Press LOAD ADDR.

4. Press START

The test will then begin, setting a binary count of successful passes on Test Console LEDs LD0-LD7.

2. PAGED MEMORY TEST

Operation with Terminal

1. Type in SE002, followed by 'CR'.

The message

NO. PAGES?

is output.

2. Type in the required number of pages, followed by 'CR'

The message

FIRST PAGE NO.?

is output.

3. Type in the number of the lowest page to be tested, followed by 'CR' .

The message

TEST NO.?

is output.

The test numbers are:-

0	Do all tests in sequence
1	Memory Write Lock Check
2	Page Register Check (Unique pages)
3	Clear all bits, Set all bits.
4	Count.
5	Checker-board pattern.
6	Address/Data Line Check.
7	Pattern.
8	Immediate Write / Read verify.
9	Pattern across pages.

4. Type in the number of the required test, followed by 'CR' .

The test then runs.

Successful completion of the selected test is indicated by the 'END OF PASS 01' message, after which the test starts again.

If required, the following options may be selected:

1	Loop on Error
2	Halt after the first pass.
3	Test memory pages at addresses other than $4000 - $4FFF.
4	Use a page register at an address other than $5000.

To select any of the above options, type N'CR' in response to the request 'NO. PAGES?'. For example:

Response	Type in	
*	SE002 'CR'	
NO PAGES?	N 'CR'	
MEM BASE ADD?	6000 'CR'	Beginning of a special 4K paged area. To test memory at $4000 -$4FFF enter 4000 'CR'.
PAGE REG ADD?	8000 'CR'	Page register address of above area. To use the normal page register address type 5000'CR'.
LP ON ERR?	Y 'CR'	Yes - loop on error (type N 'CR' for No).
HLT AFT 1ST PASS?	Y 'CR'	Do 1 pass only (type N 'CR' for No).
NO. PAGES?	4 'CR'	
1ST PAGE NO?	1 'CR'	
TEST NO?	1 'CR'	etc.

Note: Loop on error does not re-test the location but merely writes and reads it continuously to aid checking with an oscilloscope.

Operation without terminal

1. Load the number of pages to be tested into location $F608 (see section 3.1 of the 6809 TEST CONSOLE OPERATORS HANDBOOK).

2. Load the first page number to be tested into location $F609.

3. Select the required Test No. 0 - 6 (binary) on the T/C switches SW0 - SW4.

4. Select Halt after First Pass/No Halt on T/C switch SW13.

   0 - (down) = Halt

   1 - (up) = Continue

5. Select Loop on Error/No loop on T/C switch SW14.

   0 - Loop on error

   1 - Continue

6. Select special memory if required on T/C switch SW15.

0 = Galaxy Memory ($4000-$4FFF, Page Register $5000).
1 = Special Memory (4K pages)

If 'Special Memory' is selected the first address of the 4K pages should be loaded into location $F600 and the Page Register Address into location $F606.

7. Start the Program from address $E002.

3. UNPAGED MEMORY TEST

Operation with terminal

1. Type in SE004, followed by 'CR' .

   The message

   START ADDR

   is output

2. Type in the address of the lowest R.A.M. location to be tested, followed by 'CR' .

   The message

   END ADDR

   is output

3. Type in the address of the highest R.A.M. location to be tested, followed by 'CR'.

   The message

   LP ON ERR?

   is output

4. Type in Y 'CR' if the test is to loop if an error is found; or N 'CR' if the test is to continue after finding an error.

   The message

   HLT AFT 1ST PASS?

   is output

5. Type in Y 'CR' if the test is to run only once; or N 'CR' if the test is to run continuously.

   The message

   TEST NO.?

   is output

6. Type in the number of the required test (0-6,as for the Processor R.A.M.

Test), followed by 'CR' .

The test then runs, outputting END OF PASS messages as appropriate.

Operation without terminal

1. Load the Start Address into location $F600/1.

2. Load the End Address (last address tested) into $F602/3.

3. Select Loop on Error/No loop on T/C switch SW14.

   0 (Down) = Loop

   1 (Up) = Continue

4. Select Halt after first pass/no halt on T/C switch SW13.

   0 = Halt

   1 = Continue

5. Select Test No. (0 - 6) on T/C switches SW0 - SW7. These are the same as for the Processor R.A.M. test.

6. Start TMEM from address $E004.

4.TEST CONSOLE SWITCH DATA MEMORY TEST

This test uses data from the T/C switch register. Switches SW8 - SW15 define the data written to each location. LEDs LD8 - LD15 show the data read from each location.

To run the test:

1. Load first address to be tested into $F600/1.

2. Load Last address to be tested into $F602/3.

3. Start TMEM from $E006.

ERROR REPORTING

If a failed R.A.M. location is found, the TMEM tests will indicate this:-

Tests 1 and 3. (Processor R.A.M. test and Unpaged Memory test.)

The Test Console ADDRESS window displays the failed R.A.M. address.

The Test Console DATA window displays the erroneous data read from the failed address.

The terminal (if fitted) displays the heading:

MEM ERR (TEST, ADDR, BAD DATA, DATA)
followed by a line of digits.

TEST - The subtest in progress.

ADDR - The address of the failed location.

BAD DATA - The data read from the failed address.

DATA - The data originally written to the failed address.

Test 1 will then 'loop' on the failed address.

Test 3 may be selected to not loop on error, in which case a subsequent error will cause the Test Console displays to update, and additional lines of error message data to appear on the terminal.

Test 2. (Paged Memory test.)

The error reporting is similar to that for Test 1 and 3 except that the failed Page Number is displayed in binary on Test Console LEDs L8 - L15, and as an additional column in the data displayed on the terminal.

Two further error messages are possible:

LOCK ERR, PAGE 01

PAGE ERR, PAGE 01

A 'lock error' on a memory page indicates that R.A.M. access has apparently been possible after the 'write inhibit' bit has been set.

A 'page error' on a memory page indicates that either a page is not responding correctly to its number in the 'page register', or that a R.A.M. location returned incorrect data during the page register test.

Test 4. (Test Console Switch Data Memory test.)

The failed address and data are shown as for Tests 1 - 3.

Test Console LEDs L0 - L7 display those data bits which are in error.

Any test may be aborted at any time by Restart Console. Following this, the Paged and Unpaged tests may be re-entered by using a start address of $E009.

GBEXTST-A1 (Galaxy Back-up Executive Test)

This program is stored in a PROM which uses a start address of $E800.

The test will check the V.D.U. drive circuitry on the Back-Up Executive Processor, and the Back-up panel contacts, mimics and faders - via channel processor 0.

The test has four sections:

Test 0 - V.D.U. Test 0.

This outputs, to the whole V.D.U. screen, each video character in turn.

Test 1 - V.D.U. Test 1

This continuously outputs the video characters in order, to the V.D.U. screen. At every ten characters the V.D.U. attribute changes.

Test 2 - V.D.U. Test 2

This scans Test Console switches SW0 - SW7 and continuously outputs, to the whole V.D.U. screen, the character and attribute set on the switches.

For details of character and attribute codes, see instructions for TVDU, V.D.U. test program.

Test 3 - Contacts and Mimics Test

This scans the Back-up keyboard contacts and faders. Each push operated will indicate on the Test Console, and V.D.U., and may toggle an appropriate mimic. The fader levels are also displayed.

To run the tests

1. Set up the Test Console with the GBEXTST-A1 PROM in the I.C.2 slot of the test PROM card.

2. Reset the system in 'console mode' i.e. Restart Console.

3. Press START

4. Enter the desired test number on the Test Console keypad.

Tests 0 and 1 then run with no further action.

Test 2 requires appropriate settings to Test Console switches SW0 - SW7. The settings may be changed while the test is running.

Test 3 will start by illuminating all push lamps on the Back-up keyboard, and displaying the current fader levels on the V.D.U. and Test Console LEDs.

Time Fader	-	V.D.U. bottom left, LD8 - LD15.
Master Fader	-	V.D.U. bottom right, LD0 - LD7.

Depressing any push will then cause an appropriate mimic (if any) to toggle, a relevant number to appear on the V.D.U., and the same number to appear in the Test Console data display. This display will show the last push pressed if several are operated together. A table of the contact/mimic numbers is shown overleaf.

Number	Contact	Mimic	
00	0	0	)
01	1	1	) These display
02	2	2	) on the numeric
03	3	3	) display, shifting
04	4	4	) right to left as
05	5	5	) further contacts
06	6	6	) are made.
07	7	7	)
08	8	8	)
09	9	9	)
0A	FULL	Successive blanks to above	
0B	@	@	
0C	+	:	
0D	-	-	
0E	+1	n/a	
0F	THRU	THRU	
10	NEXT	Time Decimal Point	
11	TIME	TIME	
13	CLEAR	n/a	
14	.	Mem No Decimal Point	
15	ON	ON	
16	FADE DOWN	n/a	
17	FADE UP	n/a	
18	MEM	MEM	
19	CHANS S	CHANS S	
1A	CHANS P	CHANS P	
1B	PAGE	n/a	
1C	OUTPUT V.D.U.	n/a	
1D	PRESET V.D.U.	n/a	
1E	MEM V.D.U.	n/a	
1F	N/U	n/a	
20	NOT FITTED	n/a	
21	N/U	n/a	
22	REC PRESET	REC PRESET	
23	REC O/P	REC O/P	
24	N/U	n/a	
25	N/U	n/a	
26	N/U	n/a	
27	N/U	n/a	
28	SEQ	SEQ	
29	PRES MEM TRANS	PRES MEM TRANSFER	
2A	O/P MEM TRANS	O/P MEM TRANSFER	
2B	MOVE FADE	MOVE FADE	
2C	CROSSFADE	CROSSFADE	
2D	N/U	n/a	
2E	N/U	n/a	
2F	N/U	n/a	
30	MAGIC SWITCH 1	n/a	
31	MAGIC SWITCH 2	n/a	
32	MAGIC SWITCH 3	n/a	
33	MAGIC SWITCH 4	n/a	
34	MAGIC SWITCH 5	n/a	
35	MAGIC SWITCH 6	n/a	
36	MAGIC SWITCH 7	n/a	
37	MAGIC SWITCH 8	n/a	

N/U = Not used. n/a = none applicable

GBCPTST-A1 (Galaxy Back-up Channel Processor Test)

This program is stored in a PROM which uses a start address of $E800.

A terminal should be connected to the Test Console.

The test will check the basic operation and R.A.M. of a Galaxy Back-up Channel Processor.

The test is in two sections.

Test 1 - R.A.M. Test

This allows checking of the Channel Processor R.A.M. via either the EXEC register or the DMA (disc) register (or both).

Test 2 - CP Program

This writes a simple program into the CP R.A.M. and runs it. The program writes a pattern into the remaining CP R.A.M. The Executive then verifies that the program has completed and that the pattern is correct.

To run the tests

1. Remove the Disc Processor and Interface PCB from the Back-up Unit.

2. Connect the Test Console to the Back-up Executive Processor (32K Processor & Video).

3. Set up the Test Console with the GBCPTST-A1 PROM in the I.C.2 socket of the Test PROM card.

4. Reset the system in 'console mode' i.e. Restart Console.

5. Press START.

6. Enter either 1 or 2 on the Test Console keyboard to specify the required test.

   Test 1

   The message

   GB CP TEST 1
   SET SWITCHES. TYPE H OR G

   is output

   The Test Console switches SW0 - SW15 must be set to specify various possible options. These options will be listed on the terminal if H is typed. (H = HELP)

The HELP listing is as follows:-

SW #	FUNCTION
0	TEST CP 0
1	TEST CP 1
2	TEST THRU EXEC PORT
3	TEST THRU DISC PORT
4	SUPPRESS PASS REPORTING
5	SUPPRESS ERROR REPORTING
6	LOOP ON ERROR
7	WRITE IMMEDIATE READ
8	PATTERN SLIDE
15	HALT TESTING

SW0,1 Specify the CP(s) to be tested.

SW2,3 Specify the port(s) to be used for the testing. Both may be specified, in which case each check runs twice.

SW4,5 Specify information that is not to be output to the terminal.

SW6 If set, will cause the program to loop on a failed R.A.M. location.

SW7 If set, will cause an immediate read/verify after each write, rather than allowing all R.A.M. to be written before reading.

SW8 If set, will cause the data pattern to shift by one R.A.M. location after each pass.

SW15 If set, will cause the test to stop. De-setting the switch will allow the test to continue.

(Switch UP = Set, Switch DOWN = not set).

If G is typed, the test will commence, and will repeat until stopped.

Test 2

The message

GB CP TEST 2
SET SWITCHES. TYPE H OR G

is output

Again, Test Console switches SW0 - SW15 must be set, before typing G.

The HELP listing is as follows:-

SW #	FUNCTION
0	TEST CP 0
1	TEST CP I
2	TEST THRU EXEC PORT
3	TEST THRU DISC PORT
4	SUPPRESS PASS REPORTING
5	SUPPRESS ERROR REPORTING
6	LOOP ON ERROR
15	HALT TESTING

If test numbers other than 1 or 2 are entered, the message

NO TEST EXISTS

is output

Or, for test 3 the message

TEST NOT YET IMPLEMENTED

is output

ERROR REPORTING

If a data error is detected, this will be reported on the terminal (unless SW5 is set).

The heading

ERR CP PRT ADDR DI D0

is output

following by error data.

ERR A count which increments as successive errors are detected.

CP 0 or 1, to identify the failed C.P.

PRT D or E, to identify the access port (disc or exec) used during the test.

ADDR The address of the failed location. The address is calculated and given with reference to the CP address map.

DI The data written to the failed location.

D0 The data read from the failed location.

n.b. Errors occurring between C.P. addresses $1B80 and $1BFF will not be reported to prevent confusion from the C.P. communications area mapped onto these addresses.

Test 2 will not test the program storage area at the top of C.P. R.A.M.

Test 2 will output the message

CP n TIMEOUT

If a Channel Processor (identified by number n) does not complete its program within the time allowed.

FDTEST-A3 (Floppy Disc Test)

This program is stored in a PROM which uses a start address of $E800.

A terminal should be connected to the Test Console.

The test will check a Floppy Disc system.

Note: If the Disc Unit uses a 1700/F, 1707 card set, the 'SYNC RESET' link on the ref 1700/F must be cut, in order for the test to run correctly.

Two sections are contained in the test:

1. Contacts and Mimics Test (Test 0).

   This allows checking of the Disc Unit front panel contacts and mimics.

   n.b. The V.D.U. routing switch on a Galaxy Memory Back-Up is a hardware only contact and will not be checked by the test.

2. Disc Test (Tests 1,2,3)

   These tests have eleven subtests and will check disc interface and control circuitry, disc drives, and floppy discs.
   In order to achieve correct results when using Disc Tests, it is important that a properly 'formatted' disc is placed in the drive under test. It is normal to format the disc in this drive before commencing testing.

Test 1 This is used for testing a Ref.1735 disc processor card, or ref 1700/F, Ref 1707 set, in either a Galaxy Disc Unit or a Memory Back-up Disc Unit. This may be fitted with either a Western Digital FD1771 or FD1791 floppy disc controller chip (depending upon the PCB issue status).

Test 2 This is used for testing a Ref.1735 disc processor card controlling the Gemini 3.5 inch disc drive. There is no operational difference between Tests 1 and 2, but the 3.5 inch disc has 80 tracks and 16 sectors, whereas the 8 inch disc has 77 tracks and 26 sectors. Test 2 uses a stepping rate of 20ms, the standard Gemini Disc stepping rate.

Test 3 This is as Test 2 but it uses a stepping rate of 12ms with the original FD1771 disc controller chip fitted, or one of 6ms with the FD1791 disc controller chip fitted. This test provides a method of testing the Gemini Disc Unit in the event of any future changes in the stepping rate.

To run the tests

1. Remove the 32K Processor and Channel Processors from the Disc Unit (if it is a Galaxy Memory Back-up).

2. Set up the Test Console with the FDTEST-A3 PROM in the I.C.2 slot of the Test PROM card.

3. Reset the unit in 'console mode' i.e. Restart Console.

4. Press START.

5. Enter 0,1,2, or 3 on the Test Console keyboard to specify the required test.

The selected test will then be activated.

TEST 0 Contact and Mimic Test

The terminal will display the message:

THIS IS TEST 0 (GALAXY BACKUP CONTACTS AND MIMICS)

All the front panel mimics will then be illuminated. Depressing any contact will toggle the equivalent mimic (apart from DISC CLEAR).

Switching the keyswitch to REC LOCK and off again will toggle the DISC SAFE mimic.

Holding down the DISC CLEAR contact and switching the keyswitch to DISC CLEAR and off again will toggle the DISC CLEAR mimic. The POWER ON mimic will toggle every time any contact is made.

TEST 1,2,3 Floppy Disc Tests

The terminal will display a message indicating which test has been selected:

THIS IS TEST 1 (GALAXY 8 INCH DISC DRIVE TEST)

THIS IS TEST 2 (GEMINI 3.5 INCH DISC TEST, 20 MS)

THIS IS TEST 3 (GEMINI 3.5 INCH DISC TEST, 6 MS)

Following this, the operation of the tests is identical.
The disc drive motor will be switched off.
The program will then scan the console keyboard, the START contact, and the LOAD ADDRESS contact.

The keypad can be used to 'dial up' a track and sector number to be used in the tests. The track and sector number will appear in the Address window. The left byte is the track number, and the right byte is the sector number.
It is only necessary to enter track and sector numbers if they are actually required during the testing. (see subtests 13-10)

The subtests and options, required to be used, must now be selected on console switches SW15-SW0 - setting a switch to '1' (up) selects the associated option.

The tests and options selected by the switches are as follows:

SW15. Restore, no verify.
This test will issue a restore command (move disc head to track 00)to the selected drive. On completion, the disc status is displayed on Test Console LEDs LD8-LD15.

SW14. Restore and verify
This test will issue a restore command to the selected drive, followed by a verify operation. On completion, the disc status is displayed on Test Console LEDs LD8-LD15.

SW13. Seek, no verify.
This test will issue a seek command to the track number selected on the keypad. On completion, the disc status is displayed on Test Console LEDs LD8-LD15.

SW12. Seek and verify.
This test will issue a seek command to the track number selected on the keypad, followed by a verify operation. On completion, the disc status is displayed on Test Console LEDs LD8-LD15.

SW11. Read Sector
This test will attempt to read the sector selected on the keypad into a RAM buffer at $F000 to $F07F. No seek operation is performed; the read will fail if a seek command to the correct track has not been previously issued to the drive. On completion, the disc status is displayed on Test Console LEDs LD0-LD7.

SW10. Write Sector

This will attempt to write the data in the RAM buffer at $F000 to $F07F into the sector selected on the keypad. No seek operation is performed; the write will fail if a seek command to the correct track has not been previously issued to the drive. On completion, the disc status is displayed on Test Console LEDs LD0-LD7.

SW9. Not used.

SW8. Not used.

SW7. Seek Test 1
This test will carry out a series of seek and verify operations to tracks 0, 1, 2, 3 .... 75, 76, 77, 0, 77, 76, 75 .... 2, 1, 0.

SW6. Seek Test 2
As seek test 1, but tracks 0, 76, 1, 75, 2, 74 .... 75, 1, 76, 0.

SW5. Seek Test 3
As seek test 1, but tracks 45, 13, 58, 26, 71, 39 .... 32, 0 (i.e. steps of 45 modulo 77).

SW4. Surface Test-Read
This test will attempt to read every sector on the disc.

SW3. Surface Test-Write
This test will attempt to write to every sector on the disc.

SW2. If 'up', will cause the selected tests to repeat (until SW2 detected as 'down' or Restart is operated.
If 'down', will cause the program to cease testing when all selected tests have completed. The drive motor will be switched off and the program will scan the START and LOAD ADDRESS contacts.

SW1. If 'up', the detection of an error during the testing will cause the program to halt after reporting the error on the console displays.
If 'down', any errors will be reported - on the console displays, and on the terminal - but the test will continue.

SW0. 'Down' selects Drive 1
'Up' selects Drive 2

Pressing START will then cause the program to switch on the drive motor and carry out the tests as selected on the switches SW15-SW3 - starting from 15, to 3.

Tests 10 and 3 write to the disc. To prevent this happening accidentally, these tests will not be carried out unless LOAD ADDRESS is held down when START is depressed.

During the tests, the status of restore and seek operations is displayed on Test Console LEDs LD8-LD15 and the status of read and write operations is displayed on Test Console LEDs LD0-LD7. The number of the test in progress is displayed in the DATA window in hexadecimal. The number of the track under test is displayed as the left byte in the ADDRESS window, with the number of the sector under test displayed as the right byte.

ERROR REPORTING

Tests 7-3 will indicate errors, depending on the position of switch 1. If switch 1 is up, the test will halt: the erroneous track and sector will be displayed in the address window, and the erroneous status will be displayed in LEDs LD8 - LD15 for a seek error, and LD0 - LD7 for a read or write error. The test will continue if RESUME is pressed. If switch 1 is down, the error will be displayed on the terminal and the test will continue.

Terminal error messages are displayed as:- (for example)

READ ERROR TRACK 41 SECTOR 1A STATUS 08

or

WRITE ERROR TRACK 41 SECTOR 1A STATUS 08

or

SEEK ERROR TRACK 41 SECTOR 1A STATUS 10

Indicating the type of error - failure to find/read/write a particular sector on a particular track - together with the failed sector and track, and the disc 'status' at the time.

n.b. Errors on high numbered tracks (above $35) can normally be ignored. It is extremely unlikely that such tracks will be recorded during normal disc usage.

Status bit meanings are given below:-

For Seek or Restore commands:-

LD15 D7	Disc not ready - door open?
LD14 D6	Disc write protected.
LD13 D5	Head engaged.
LD12 D4	Seek error.
LD11 D3	CRC error. (Cyclic Redundancy Check error)
LD10 D2	Head is at track 0.
LD9 D1	Index mark detected.
LD8 D0	Disc busy - probably timed out - door open?

For Read or Write commands:-

LD7 D7	Disc not ready - door open?
LD6 D6	On read = 0, On write, disc write protected - or attempting tests 10 or 3 without depressing LOAD ADDRESS.
LD5 D5	On read = 0, on write, write fault. (not used)
LD4 D4	Correct track and sector ID not found.
LD3 D3	CRC error.
LD2 D2	Data missed.
LD1 D1	Data request detected.
LD0 D0	Disc busy - probably timed out - door open?

For further information, refer to the Western Digital FD1771 Floppy Disc Controller data sheet.

USAGE OF SUBTESTS

15,14 Restore / Restore and Verify

All test sequences should begin with a 'Restore'.

13,12 Seek / Seek and Verify (specific track / sector)

Used when it is necessary to move the disc drive head to a specific track (and locate a specific sector within that track).
eg. when using a disc drive alignment disc, or for finding a sector prior to testing it (tests 11,10)

11,10 Sector Read / Write (specific sector)

Used for testing a specific sector on a disc.

7,6,5 Seek Tests

Used for testing disc drive head movement accuracy, head read circuitry - as track identifications are read, and for checking the accuracy of the disc 'format'.

4,3 Read / Write whole disc

Used for testing disc drive read and write circuitry, and integrity of disc recording surface.
nb. Read or Write errors will be reported if head alignment is incorrect or for a variety of other faults within the disc system.

For disc system 'exercising', subtests 14,7,6,5,4,3 are recommended (with SW2 set for continuous running and SW 1 set to continue after error)

SUMMARY OF SWITCHES 15-0

SW15	Restore, non-verify.
SW14	Restore and verify.
SW13	Seek, no verify.
SW12	Seek and verify.
SW11	Read sector.
SW10	Write sector.
SW9	Not Used.
SW8	Not Used.
SW7	Seek Test 1.
SW6	Seek Test 2.
SW5	Seek Test 3.
SW4	Read whole disc.
SW3	Write whole disc.
SW2	Repeat Tests
SW1	Halt on errors (tests 7-3)
SW0	Drive selected - '0'= Dr.1 '1'= Dr.2

APPENDIX 1

DISCONTINUED TEST PROGRAMS

The following test programs are no longer supported by Strand Lighting as current software:-

TCP - Channel Processor Test

GBEXT - Galaxy Back-up Executive Test

GBCPT - Galaxy Back-up Channel Processor Test

FDTST - Floppy Disc Test

FDTEST-A1 - Floppy Disc Test

FDTEST-A2 - Floppy Disc Test
(This may still be used - as for FDTEST-A3 - except when testing Toshiba or Y-Data disc drives).

All these programs have been superceded by improved versions.

Strand Lighting Engineering Service Department should be consulted regarding the supply of latest versions of test programs.

APPENDIX 2

USE OF 6809 TEST PROGRAMS

The following list gives guidelines as to which tests are applicable to checking the various sections of hardware contained in Strand Lighting systems using MC6809 microprocessors.

GALAXY

Ref 1700/E Executive Processor

RAM	TMEM	Test 1
PROM	TCKSM	PROM size '3' (PROM's E000, E800, F000, F800 cannot be tested in situ).

Ref 1701 Serial Interface

No applicable tests

Ref 1702 VDU Interface (Test via Executive test port)

TVDU	All tests.

Ref 1703 32K Memory (Test via Executive test port)

TMEM	Test 2 (8 pages per PCB)

Ref 1704 Channel Processor (Test via Executive test port)

CPTST 3	All tests

Ref 1705 Desk Interface

RAM	TMEM	Test 3 (addr. range 0000-0FFF)
PROM		Cannot be tested in situ

Ref 1708 Core Interface (+ core units) (Test via Executive test port)

TMEM	Test 2

Ref 1722 Program Expansion (Test via Executive test port)

RAM	TMEM	Test 3 (addr. range 2000-3FFF) (or test together with Executive RAM using TMEM Test 3 - addr. range 0000-3FFF)
PROM	TCKSM	PROM size '3'.

Ref 1732 96K Processor (Executive)

RAM	TMEM	Test 3 (addr. range 0000-3FFF)
PROM	TCKSM	PROM size '5' (PROM E000 cannot be tested in situ)

Ref 1747 Co-Processor (Remove Executive from 'bus')

RAM	TMEM	Test 3 (addr. range 0000-5FFF)
PROM	TCKSM	PROM size '5' or '6' (PROM E000/C000 cannot be tested in situ) (exact configuration depends on program version).

Ref 1751 Multiplex Channel Processor (Test via Executive test port)

RAM	CPTST 3	Test 1,2 Also tests DMA circuitry. (To test processor operation and output circuit use 'on-board' tests).

Ref 1771 64K Memory. (Test via Executive test port).

	TMEM	Test 2 ($10 pages per PCB)

GALAXY DISC AND MEMORY BACK-UP

Ref 1700/F Disc Processor (Executive)

Test as Ref 1700/E.

Ref 1707 Disc Interface (Test via Executive test port).

Cont. I/F	FDTEST-A3	Test 0
Disc I/F	FDTEST-A3	Test 1
RAM		Not normally fitted

Ref 1735 Disc Processor and Interface

RAM	TMEM	Test 1
PROM	TCKSM	PROM size '5' (PROM E000 cannot be tested in situ)
DISC I/F	FDTEST-A3	Test 1

Ref 1734 32K Processor and Video (Executive)

RAM	TMEM	Test 1
PROM	TCKSM	PROM size '5' (PROM E000 cannot be tested in situ)
VDU I/F	GBEXTST-A1	Test 0,1,2.

Ref 1731 Channel Processor (Test direct)

RAM	TMEM	Test 1
(Test via Executive test port)		
RAM	GBCPTST-A1	Test 1 (2)
General	GBCPTST-A1	Test 2
Contact Mimic I/F	GBEXTST-A1	Test 3

GEMINI

Ref 1732/G 96K Processor (Executive)

RAM	TMEM	Test 3 (addr. range 0000-3FFF)
PROM	TCKSM	PROM size '6' (PROM E000 cannot be tested in situ).

Ref 1702 Video Interface (Test via Executive test port)

	TVDU	All tests

Ref 1751 Multiplex Channel Processor (Test via Executive test port)

RAM	CPTST 3	Test 1,2 Also tests DMA circuitry (To test processor operation and output circuit, use 'on-board' tests)

Ref 1752 Serial, Memory, Terminator (Test via Executive test port)

RAM	TMEM	Test 2 (8 pages, 1st page 0)

Ref 1735/M Disc Processor and Interface

RAM	TMEM	Test 1
PROM	TCKSM	PROM size '6' (PROM E000 cannot be tested in situ)
	Disc I/F	FDTST-A3 Test 2 (Test 3 may be required depending on disc drive type).

Ref 1749 Memory and Submasters Panel (Panel I/F)

RAM	TMEM	Test 3 (addr. range 0000-0FFF)
PROM		Cannot be tested in situ.

M24

Ref 1832 and Ref 1833 Motherboard and Front Panel

M24 system tests should be used.

Ref 1857 Effects Processor

RAM	TMEM	Test 3 (addr. range 0000-07FF)
PROM		Cannot be tested in situ.

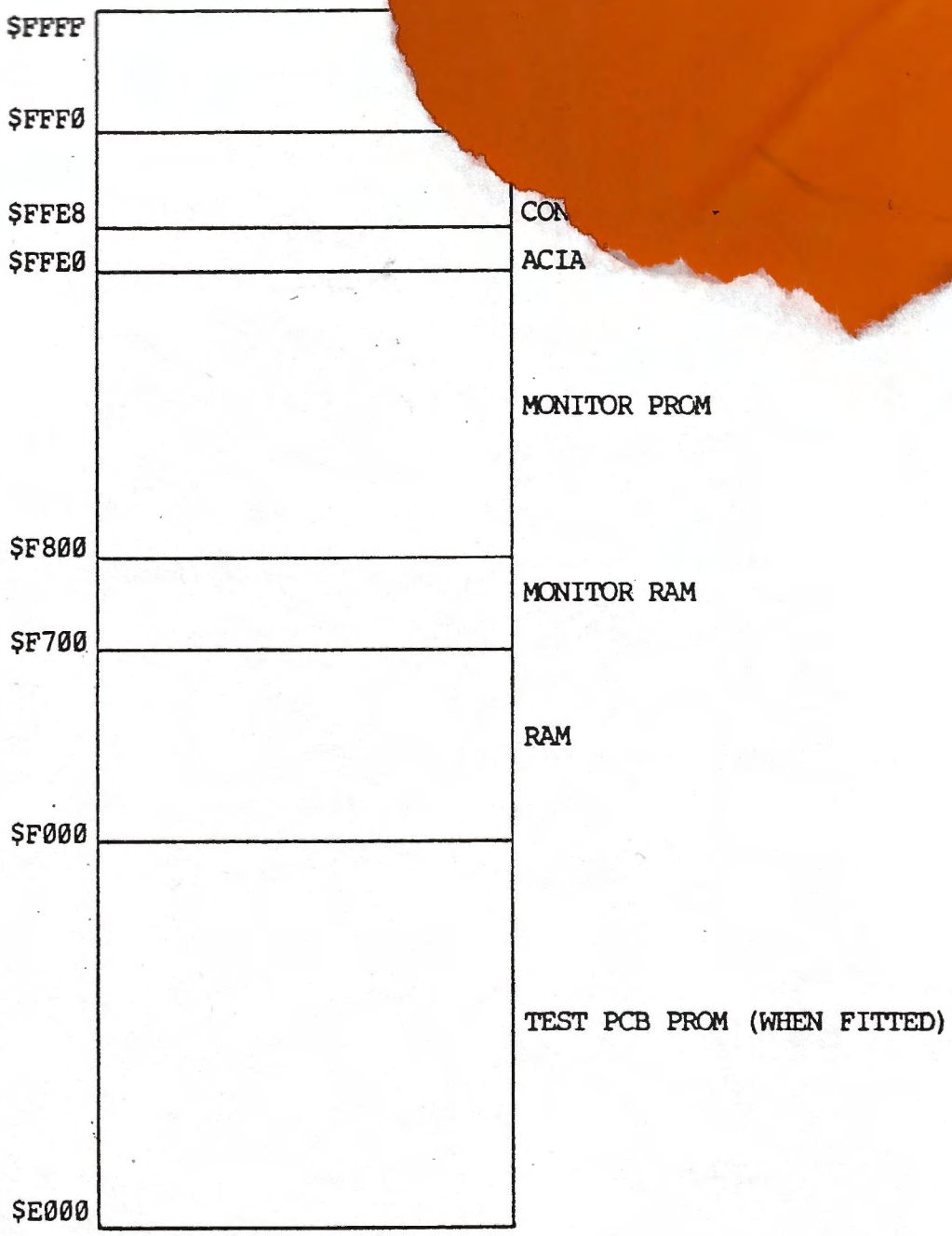
ACTION

RAM	TMEM	Test 3 (addr. range 0000-3FFF)
PROM		Cannot be tested in situ.

LIGHTBOARD M

No test port fitted	T/C cannot be connected.

ADDRESS OVERLAY.



Strand Lighting