STRAND

TEMPUS M24

MEMORY LIGHTING CONTROL

MAINTENANCE HANDBOOK

TECHNICAL INFORMATION

Rank Strand Limited PO Box 51 Great West Road Brentford Middlesex TW8 9HR Telephone 01 568 9222 Telex 27976
Cables Rankaudio Brentford

Rank Strand

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MEMORY LIGHTING CONTROL

MAINTENANCE HANDBOOK

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A company within the Industrial Division of The Rank Organisation Limited

Rank Strand

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CONTENTS

CHAPTER 1 - INTRODUCTION

1.1	GENERAL	1
1.1.1	Patch/Effects System	2
1.2	CONSTRUCTION	2
1.2.1	Control Console	2
1.2.2	Multiplex Interface Unit	3
1.2.2.1	Connections	4
1.2.3	M24Fx Patch/Effects Unit	4
1.2.3.1	Connections	5
1.3	SPECIFICATION	5
1.4	USING THE HANDBOOK	8
1.4.1	Glossary of Terms	8

CHAPTER 2 - SYSTEMS DESCRIPTION

2.1	INTRODUCTION	1
2.2	CONTROL CONSOLE	1
2.2.1	Power Supplies	1
2.2.2	Panel Board	1
2.2.2.1	Address Map	2
2.2.2.2	Panel Processor Program	4
2.2.3	Motherboard and Executive Processor	7
2.2.3.1	Address Map	7
2.2.3.2	Panel Communication Interface	8
2.2.3.3	Tape Interface	9

2.2.3.4 Analogue Interface 9
2.2.3.5 Motherboard Processor Program 11
2.2.4 Panel/Motherboard Communication 13
2.2.4.1 Communication Format 14
2.2.4.2 Control Bytes 14
2.2.4.3 Sync Byte 15
2.2.5 Video Interface 15
2.3 MULTIPLEX INTERFACE UNIT 18
2.3.1 Channel Demultiplexer 18
2.3.2 Channel Multiplexer 19
2.3.3 Independent Operation 19
2.4 M24Fx PATCH/EFFECTS UNIT 19
2.4.1 Power Supplies 19
2.4.2 Effects Processor Board 20
2.4.2.1 Address Map 20
2.4.2.2 Patch Master Faders 22
2.4.2.3 Effects System 22
2.4.2.4 Sync Detector 24
2.4.2.5 Effects Processor Program 24

CHAPTER 3 - CONTROL PANEL BOARD

3.1 INTRODUCTION 1
3.2 THE MICROPROCESSOR 1
3.3 PANEL PROCESSOR ADDRESSES 2
3.3.1 Program PROM 2
3.3.2 External RAM 3
3.3.3 Wheel Interface 3
3.3.4 Interrupt Latch 3
3.3.5 Address Locations within the MPU 3
3.4 SERIAL COMMUNICATIONS INTERFACE 4
3.5 DISPLAY AND PUSH-BUTTON MATRICES 4
3.5.1 Display Matrix 5
3.5.2 Button Matrix 5
3.5.3 Display and Contact Scan 6
3.6 MASTER FADERS AND FADE DURATION CONTROLS 7
3.7 RESET CIRCUIT 7

CHAPTER 4 - WHEEL INTERFACE BOARD

4.1	INTRODUCTION	1
4.2	MOVEMENT DETECTOR	1
4.3	THE COUNT PROCESS	3
4.4	COUNT LIMIT DETECTION	3
4.5	MICROPROCESSOR READ ACTION	4

CHAPTER 5 - MOTHERBOARD

5.1	INTRODUCTION	1
5.2	THE MICROPROCESSOR	1
5.3	MOTHERBOARD PROCESSOR ADDRESSES	2
5.3.1	Kernel PROM Addresses	2
5.3.2	Paged PROM Addresses (Page 0)	3
5.3.3	RAM Addresses	3
5.3.3.1	Memory Lock	4
5.3.3.2	Reset Write Inhibit	5
5.3.3.3	RAM Bus Buffers	5
5.3.3.4	Battery Circuit	6
5.3.4	Peripheral Interface Addresses	6
5.4	SYSTEM BUS INTERFACE	7
5.5	PERIPHERAL INTERFACE ADAPTER	9
5.6	PANEL COMMUNICATION INTERFACE	10
5.6.1	Transmit/Receive Clock	10
5.7	ANALOGUE INTERFACE	11
5.7.1	Multiplexed Analogue Output	11
5.7.1.1	Reference Voltage	11
5.7.1.2	Sync Pulses	11
5.7.2	Analogue Input	12
5.7.2.1	Fader Full Reference Voltage	14
5.8	TAPE INTERFACE	14
5.8.1	Transmitter Circuit	14
5.8.2	Receiver Circuit	15
5.8.3	Audio Test Circuit	17
5.9	RESET CIRCUIT	18

CHAPTER 6 - POWER SUPPLY BOARD

6.1	INTRODUCTION	1
6.2	+15V AND -15V SUPPLIES	1
6.3	+5V SUPPLY	1

CHAPTER 7 - VIDEO INTERFACE

7.1	INTRODUCTION	1
7.1.1	Principle of Operation	1
7.1.2	Video Signal	2
7.2	VIDEO INTERFACE ADDRESSES	2
7.3	VIDEO CLOCK GENERATOR	2
7.4	VIDEO SCAN	3
7.4.1	Character Line Synchronisation	4
7.5	VIDEO OUTPUT	6
7.5.1	Character Attributes	7
7.6	MPU ACCESS TO THE VIDEO SYSTEM	8
7.6.1	Loading Display Characters into the RAM	10
7.6.2	CRTC Initialisation	11
7.7	VIDEO MODULATOR BOARD	11

CHAPTER 8 - MULTIPLEX/DEMULTIPLEX BOARD

8.1	INTRODUCTION	1
8.2	MULTIPLEXED ANALOGUE INPUT	1
8.2.1	Channel Sync Pulses	1
8.2.2	Analogue Sampling	2
8.2.3	Output Enable	3
8.2.4	Dimmer Drive Outputs	6
8.2.5	Frame Sync	6
8.3	MULTIPLEXED ANALOGUE OUTPUT	7
8.3.1	Analogue Inputs	7
8.3.2	Multiplexed Output	7
8.3.3	Output Disable	8
8.3.4	MUX OK Indicator	8
8.4	CHANNEL COUNTER	10
8.4.1	Card Enable	12
8.5	INDEPENDENT OPERATION	12

8.5.1	Free-run Oscillator	13
8.6	POWER-UP INHIBIT	14
8.7	POWER SUPPLIES	15
8.7.1	Detailed Circuit Description	16

CHAPTER 9 - EFFECTS PROCESSOR BOARD

9.1	INTRODUCTION	1
9.2	THE MICROPROCESSOR	1
9.3	EFFECTS PROCESSOR ADDRESSES	1
9.3.1	Program PROM	2
9.3.2	Alpha-numeric Display	3
9.3.3	Peripheral Interface Adapters	3
9.3.4	Random Access Memory	3
9.3.4.1	Battery Circuit	4
9.4	PANEL INTERFACE	4
9.4.1	Button Matrix	4
9.4.2	Indicators	5
9.5	PATCH MASTER FADERS	5
9.5.1	Master Level Indicators	6
9.6	EFFECTS SYSTEM	6
9.6.1	Effects Master Fader	7
9.6.2	Chaser	7
9.6.3	Flash Generator	8
9.6.4	Sound-to-light Generator	8
9.6.4.1	Random Flicker	9
9.6.5	Flash Buttons	9
9.7	SYNC DETECTOR	9
9.7.1	Normal Operation	10
9.7.1.1	Frame Sync Separator	11
9.7.1.2	Multiplex Detector	11
9.7.1.3	Sync Interrupt	13
9.7.2	Operation in Back-up Mode	13
9.7.2.1	Sync Generator	14
9.7.2.2	Local Frame Sync	14
9.7.2.3	Entering Back-up Mode	15
9.8	CHANNEL 'ON' DETECTOR	16
9.8	RESET CIRCUIT	16

CHAPTER 10 - SERVICING AND MAINTENANCE

10.1 INTRODUCTION	1
10.1.1 Equipment Required	1
10.1.2 General Cautions	2
10.1.2.1 Power	2
10.1.2.2 Proms	2
10.1.2.3 Printed Circuit Boards	2
10.1.2.4 Handling CMOS Integrated Circuits	2
10.1.2.5 Food and Drink	3
10.1.2.6 Control Panels	3
10.2 INITIAL SETTING-UP	3
10.2.1 Panel Board (Ref. 1833)	4
10.2.2 Motherboard (Ref. 1832)	4
10.2.3 Wheel Interface Board (Ref. 1706)	6
10.2.4 Video Interface (Ref. 1834)	6
10.2.5 Console and M24Fx Power Supply Units	7
10.2.6 Multiplex/Demultiplex Board (Ref. 1828)	7
10.2.7 Effects Processor Board (Ref. 1857)	8
10.3 ROUTINE SERVICING	9
10.3.1 Weekly	10
10.3.2 Quarterly	10
10.3.3 Yearly	10
10.4 POWER SUPPLIES	11
10.4.2 Fuses	12
10.4.2.1 Control Console	12
10.4.2.2 Multiplex Interface Unit	12
10.4.2.3 M24Fx	12
10.5 REMOVAL AND REFITTING OF SUB-ASSEMBLIES	12
10.5.1 Control Console	13
10.5.1.1 Preliminary	13
10.5.1.2 Power Supply Unit	13
10.5.1.3 Video Interface	13
10.5.1.4 Motherboard	14
10.5.1.5 Panel Board	15
10.5.1.6 Channel Control Wheel	16
10.5.2 Multiplex Interface Unit	16
10.5.3 M24Fx	16

10.5.3.1 Preliminary 16
10.5.3.2 Power Supply Unit 18
10.5.3.3 Panel Board 18
10.6 TEST PROGRAMS 18
10.6.1 Power-up Self Tests 19
10.6.2 Panel Tests 19
10.6.2.1 Test 1 - Display Test 20
10.6.2.2 Test 2 - Contact Test 20
10.6.2.3 Test 3 - Communication Test 20
10.6.2.4 Test 4 - Program Test 21
10.6.2.5 Test 5 - Select System Tests 21
10.6.3 System Tests 22
10.6.3.1 VDU Test (A) 23
10.6.3.2 VDU Test (B) 23
10.6.3.3 Master and Time Faders 24
10.6.3.4 Tape Interface 25
10.6.3.5 Program Checksum 25
10.6.3.6 Cue Store 25
10.6.3.7 Analogue Interface 26
10.6.4 Returning to Normal Operation 26

DRAWINGS

7B26998	Issue C	Desk Wiring Diagram	
6A26904	Issue E	Panel Board, circuit diagram	Ref.1833
6B24310	Issue 3	Wheel Interface, circuit diagram	Ref.1706
6A26932	Issue E	Motherboard, circuit diagram (2 sheets)	Ref.1832
7C26933	Issue B	Power Supply Unit, wiring diagram	
6C26865	Issue D	Power Supply Board, circuit diagram	Ref.1830
6A26940	Issue C	Video Interface, circuit diagram	Ref.1834
6C28009	Issue C	Modulator Board, circuit diagram	Ref.1839
7B26872	Issue C	Multiplex Interface Unit, wiring diagram	
6A26850	Issue D	Mux/Demux Board, circuit diagram	Ref.1828
7C28189	Issue B	M24Fx Wiring Diagram	
6A28128	Issue E	Effects Processor Board, cct. dia. (2 shts)	Ref.1857
6C28178	Issue A	Power Supply Board, circuit diagram	Ref.1863

CHAPTER 1

INTRODUCTION

1.1 GENERAL

Tempus M24 is a new, compact, memory lighting control system which is intended for use in installations which would previously have been served by a manual system. It offers many of the sophisticated facilities previously available only on much more expensive systems and has an added advantage in that it often may be incorporated in an existing manual system with the minimum of rewiring.

The basic system consists of two units: a Control Console and a 24-way Multiplex Interface unit which produces the dimmer control signals. Additional Multiplex Interface units may be added for systems with more than 24 lighting channels.

In addition to producing dimmer control outputs, the Multiplex Interface unit may accept inputs from another lighting control system, e.g. a Tempus or AMC desk. The contribution from the second system combines with the M24 output on a 'Highest-takes-precedence' basis and may be controlled by a MANUAL master on the M24 console and recorded in the M24 memories.

The number of memories available depends on the number of lighting channels, but this only affects full size, 60-channel systems which have 185 memories. Systems with fewer channels, i.e. 48, 36, 24 and 12, all have 199 memories, the maximum which can be selected on the keypad.

M24 uses battery-maintained electronic memories which will retain their data for at least a week if the system is not used. For longer term storage, the memories may be copied onto tape; most domestic cassette recorders are suitable.

A normal addition to the basic system is the Video Interface, which augments the desk indicators, etc. by producing a comprehensive

'system status' display on a standard monochrome television (not usually supplied by Rank Strand) or a video monitor. The information shown includes the current output levels of all channels, channels currently under control and fade progress.

1.1.1 Patch/Effects System

M24Fx, a simple, independently powered control system with an electronic on/off memory, is available to act as a back-up to M24. The unit includes a special effects system and it can also provide a convenient means of controlling practical circuits and working lights.

1.2 CONSTRUCTION

1.2.1 Control Console

The M24 Control Console is a desk-top unit with a removable lid, which houses the control panel and most of the system electronics. It requires a mains supply of 220/240V or 110/120V a.c. single phase (L. N. and E.), which connects via an I.E.C. 3-pin plug at the rear of the desk. Other connections are as follows:

i) Data link to the Multiplex Interface unit(s). Two core 0.5mm^2 cable with overall screen, fitted with 3-pin type XLR connectors.

ii) Connection to a tape recorder (if required). A 5-pin 180° DIN socket is provided adjacent to the Multiplexed Output connector at the rear of the desk.

iii) Output to Video Mimic. Systems provided with this optional facility have an additional connector panel at the rear of the desk. Two outputs are provided: a UHF signal to drive a standard monochrome television set (VHF is available to special order) and a composite video output for use if a video monitor is available. The television output appears on a standard co-axial connector, and the video on a 75 Ohm BNC connector.

The Control Console houses two main printed circuit boards, the Panel board (Ref. 1833) and the Motherboard (Ref. 1832). These are mounted one behind the other at the rear of the control panel. The Panel board carries the panel controls (with the exception of the channel control wheel) and is responsible for scanning the push-buttons and displays. The Motherboard is responsible for the overall control of the system and for communication with the Multiplex Interface units and the tape recorder.

Other printed circuit boards are as follows:

i) Power Supply board (Ref. 1830) - this forms part of the power supply assembly in the base of the console.

ii) Wheel Interface (Ref. 1706) - this forms part of the channel control wheel assembly on the right of the control panel.

iii) Video Interface (Ref. 1834), when fitted - this is a plug-in 'daughter' board which connects directly onto the Motherboard.

iv) Modulator board (Ref. 1839), when fitted - this board forms part of the Video connector panel at the rear of the console.

1.2.2 Multiplex Interface Unit

This is a small unit which may be placed in any convenient position. Two types are available: one intended for use with Tempus dimmer packs and control desks, and the other for use with other types of equipment (e.g. Permus dimmers and AMC control desks). Each unit provides control outputs for 24 dimmers. In installations with more than 24 lighting channels, the Multiplex Interface Units link together, so that only a single connection is necessary from the Control Console.

1.2.2.1 Connections

Each Multiplex Interface unit requires a mains input of 22Ø/24ØV or 11Ø/12ØV a.c. single phase (L. N. and E.), which connects via an I.E.C. 3-pin plug.

The data link from the Control Console connects to a three-pin XLR plug. If more than one Interface unit is used, they link together by connecting the Multiplex Output (EXTENSION O/P) socket on one unit to the MULTIPLEX I/P plug on the next.

The units for use with Tempus dimmers and control desks are fitted with four control cable tails, one for each group of six channels (i.e. 1-6, 7-12, etc.). Each cable is fitted with the necessary 8-pin in-line plug for connection to a Tempus dimmer pack. The control cable for the corresponding channels on the Tempus desk plugs into an 8-pin chassis-mounted socket above and to the left of each cable outlet.

The other type of unit has two chassis-mounted 25-way miniature D-type connectors; a socket labelled OUTPUT 1-24 and a plug labelled INPUT 1-24 for connection to the dimmers and the manual desk respectively.

1.2.3 M24Fx Patch/Effects Unit

The Tempus M24Fx Patch/Effects system is an optional addition to the Tempus M24 Memory Lighting Control. It is designed to fulfil several functions: it can act as a back-up to M24, providing simple control facilities which permit continued operation in the unlikely event of failure of the main console; it provides a suitable means of controlling house-lights, orchestra-lights, etc., for which it may be inconvenient to use the main console; and it includes an effects system which may be used for discotheques, light entertainment, etc.

1.2.3.1 Connections

M24Fx is a desk-top unit similar to the M24 Console. It requires a mains input of 220/240V or 110/120V a.c. single phase (L. N. and E. - the unit must be earthed), which connects via an I.E.C. 3-pin plug. A suitable mains lead is provided, but this must be fitted with a mains plug by the user.

There are normally also two data connections; to the M24 Console (MEMORY SYSTEM) and to the Multiplex Interface units (DIMMER I/F). Only the DIMMER I/F connection is necessary on systems where there is no M24 console. Both data connections use 3-pin type XLR connectors, a suitable cable 5 metres long being provided with both M24Fx and the M24 console; longer (25 metre) cables are available if required.

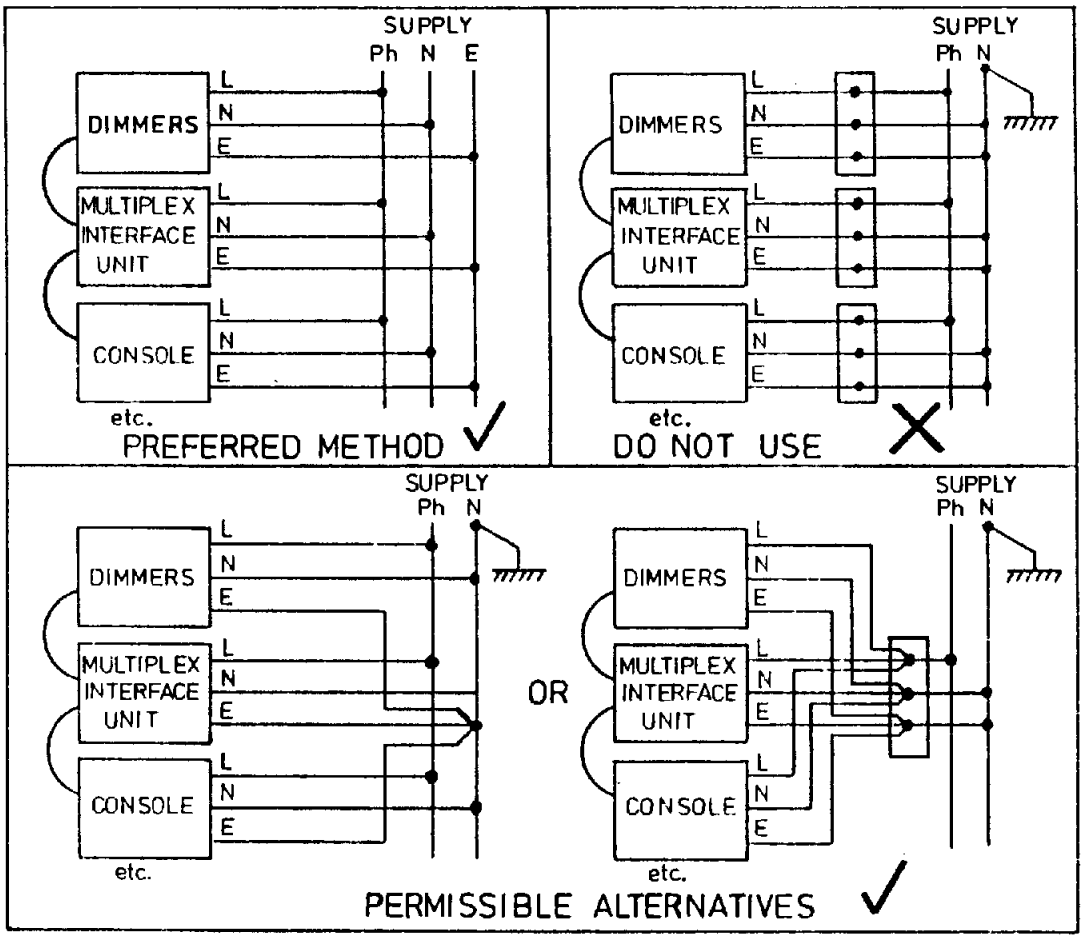
1.3 SPECIFICATION

Power input - 220V-240V or 110V-120V, 47-63Hz (specified at time of order). Each unit requires a separate power input.

WARNING: Rank Strand Tempus M24 lighting control equipment must be properly earthed if it is to function correctly. IT IS ESSENTIAL THAT EARTH BE AT THE SAME POTENTIAL AT ALL POINTS IN THE SYSTEM. If this is not the case, circulating currents may be generated in the signal earth connections, leading to fluctuating light levels and, in extreme cases, severe damage to the equipment.

In cases where the earth is provided via the supply neutral, all units (i.e. Console, Manual Fader Wing, Multiplex Interface units, Effects unit and dimmers) should ideally be powered from the same source via adequately rated three core (L. N. E.) cable. If this is not possible, a single earth point must be chosen and all the units earthed ONLY AT THIS POINT. The conductors used must be able to carry any potential fault current.

If damage is caused as a result of failure to observe the above recommendations, any warranty will be invalidated. If in doubt, your local Rank Strand agent will be pleased to advise.



Desk output - Multiplexed analogue link via 2-core screened cable.

Dimmer drive outputs (from Multiplexed Interface unit).

- ØV (Off) to -1ØV (Full) via 1Øk ohm and silicon diode.
- Optionally ØV (Off) to +1ØV (Full) via 1k ohm and silicon diode.
- Other control voltages are possible, within the limits +/-15V.

Connection is via 4 x 2m long control cables, each terminated in an 8-pin 'Bleecon' plug to mate with Tempus dimmer packs, or via a 25-way 'D' type socket.

Input from Manual Fader Desk or Wing.

- As for dimmer drive outputs.

Connection is via chassis-mounted 8-pin 'Bleecon' sockets to mate with Tempus desks, or via a 25-way 'D' type plug.

Control Channels.

- In increments of 12, from 24 to 60 maximum. One Multiplex Interface unit is required for each 24 channels.

Operating Environment.

- Temperature, 0°C to 35°C. Maximum relative humidity, 10% to 90% (non-condensing). 'Office' level cleanliness.

Processors - M6803: 8-bit data, 16-bit address.
M68B09: 8-bit data, 16-bit address.

Cycle Time - Executive: typically 48ms.
Contact scan: typically 12ms.

Fade Processing Accuracy - 16-bit.

Recording Accuracy - 8-bit (256 step).

Output Accuracy - 8-bit (256 step).

Fast Access Memory.

- Low-power semiconductor, battery-maintained for a minimum of one week.

- Number of memories available depends on number of channels fitted. 60 channel systems have 185 memories, while smaller systems have 199.

Video Mimic Output.

- Modulated monochrome UHF (optionally VHF) 625/525 line, 50/60Hz field with connection via co-axial connector, and 1V positive composite video with connection via 75 ohm BNC socket.

Tape Memory Storage

- Uses standard domestic audio recorder. 100mV rms input/output on standard 5-pin DIN socket; mono or stereo.

Dimensions - Control Console

Width	:	530mm
Depth	:	360mm
Height	:	175mm
Clearance required at rear	:	90mm
Height including lid	:	235mm
OR	:	190mm (depends on position of lid).

- Multiplex Interface Unit

Width	:	280mm
Depth	:	75mm
Height	:	200mm
Clearance required at front	:	110mm

1.4 USING THE HANDBOOK

When using this handbook, the following conventions should be noted:

i) Whenever numbers are used, they are decimal (i.e. to base 10) unless otherwise indicated. Those prefixed with a dollar ($) sign are hexadecimal (base 16).

ii) Integrated circuits are identified by their component number, prefixed with the letters IC (e.g. IC7). Where an integrated circuit contains more than one logic element, the output pin number of the element concerned is added as a suffix, e.g. IC13/4. In the case of elements with two or more outputs, e.g. bistables, one of the outputs is chosen for identification purposes, depending on the context.

iii) The term 'pin' is used to identify connections to integrated circuits. Connections to printed circuit boards are referred to as 'board terminal' or simply 'terminal'.

iv) Logic levels depend on whether the logic concerned is TTL or CMOS. In the case of TTL, >2.4V equals logic 1 and <0.8V logic 0, while CMOS levels are >3.5V for logic 1 and <1.5V for logic 0, unless the rails to the device concerned determine otherwise. Where a signal is low active, this is indicated in the text and on the circuit diagrams.

1.4.1 Glossary of Terms

The following lists abbreviations and mnemonics used in the handbook:

A0 to A15 Address Bus lines (16 bits) - A0 is the least significant bit. In the case of the 6803, A0 - A7 are multiplexed on the Data/Address bus (D0/A0 - D7/A7) and

addresses are valid on the trailing edge of 'AS'. In the case of the 69BØ9, addresses are valid on the leading edge of 'Q'.

ACIA — Asynchronous Communications Interface Adapter.

AS (68Ø3) — Address Strobe - see AØ - A15.

BA (68BØ9) — Bus Available.

BS (68BØ9) — Bus Status.

CTS — Clear to Send.

DØ to D7 — Data Bus lines (8 bits) - DØ is the least significant bit. In the case of the 68Ø3 these lines also carry multiplexed address signals. For both processors data is valid on the trailing edge of 'E'.

DMA/BREQ — Direct Memory Access/Bus Request.

E — Phase 2 timing signal - Data is latched on the trailing edge of 'E'. (See also 'Q' and 'AS').

EPROM — Erasable Programmable Read only Memory.

FIRQ (68BØ9) — Fast Interrupt Request.

HALT — Stop Processing

IRQ — Interrupt Request.

LED — Light Emitting Diode.

MRDY (68BØ9) — Memory Ready for Transfer - When MRDY is low, 'E' may be stretched, allowing the system to interface with slow memories. The stretch is by integral multiples of quarter clock cycles, up to a maximum of 1Ø micro-seconds.

NMI	Non-maskable Interrupt.
PROM	Programmable Read only Memory.
PIA	Peripheral Interface Adapter.
Q (68B09)	Quadrature Timing Signal (which leads E) - Addresses from the MPU are valid on the leading edge of 'Q'.
R/W	Read or Write - This signal indicates the direction of data transfer on the Data Bus and is low for Write. It is valid on the rising edge of 'Q' on the 68B09 and on the trailing edge of 'AS' on the 6803.
RESET/RST	Reset Signal - The RESET line is held low during the initial power-on sequence to ensure logical start-up.
RAM	Random Access Memory.
RTS	Request to Send.
Rx	Receiver circuit.
Tx	Transmitter circuit.

CHAPTER 2

SYSTEMS DESCRIPTION

2.1 INTRODUCTION

This chapter describes the function of the various parts of the system and how they interact. The printed circuit boards are only covered in broad outline. For detailed circuit descriptions see chapters 3 - 9.

2.2 CONTROL CONSOLE

The Control Console contains two main printed circuit boards: the Motherboard (which carries the Executive processor) and the Panel Board. Smaller boards form part of the Power Supply Unit (in the base of the console) and the channel control wheel. Systems with a Video Mimic have an additional board mounted directly on the Motherboard and a small board carrying the video modulator attached to the video output panel.

The Motherboard and the Panel Board each carry a self-contained microprocessor system. These exchange data by means of a serial link.

2.2.1 Power Supplies

The low voltage power supplies for the Control Console electronics are taken from a single unit mounted in the base of the console. This has outputs at +15V, +5V and -15V, and these are connected to the Motherboard; the latter distributes the power to the other boards as shown on Drawing No. 7B26998.

2.2.2 Panel Board

The Panel Board is mounted on the rear of the control panel and carries the push-buttons, faders and displays. Its microprocessor (M68Ø3) is responsible for scanning the buttons and displays and

also for reading the movement of the fader wheel. It communicates with the Motherboard processor via a serial link.

The panel faders, although mounted on the Panel Board, are not scanned by the Panel processor, but are connected directly to an analogue-to-digital converter on the Motherboard.

2.2.2.1 Address Map

The Panel processor address map is shown in Fig. 2.2.1 and described below:

i) Program PROM

The Panel Processor program is held in U.V. erasable PROM (normally 2716) located at addresses $F800 - $FFFF. Note that addresses $E000 - $F7FF are reserved for future program expansion.

ii) External RAM

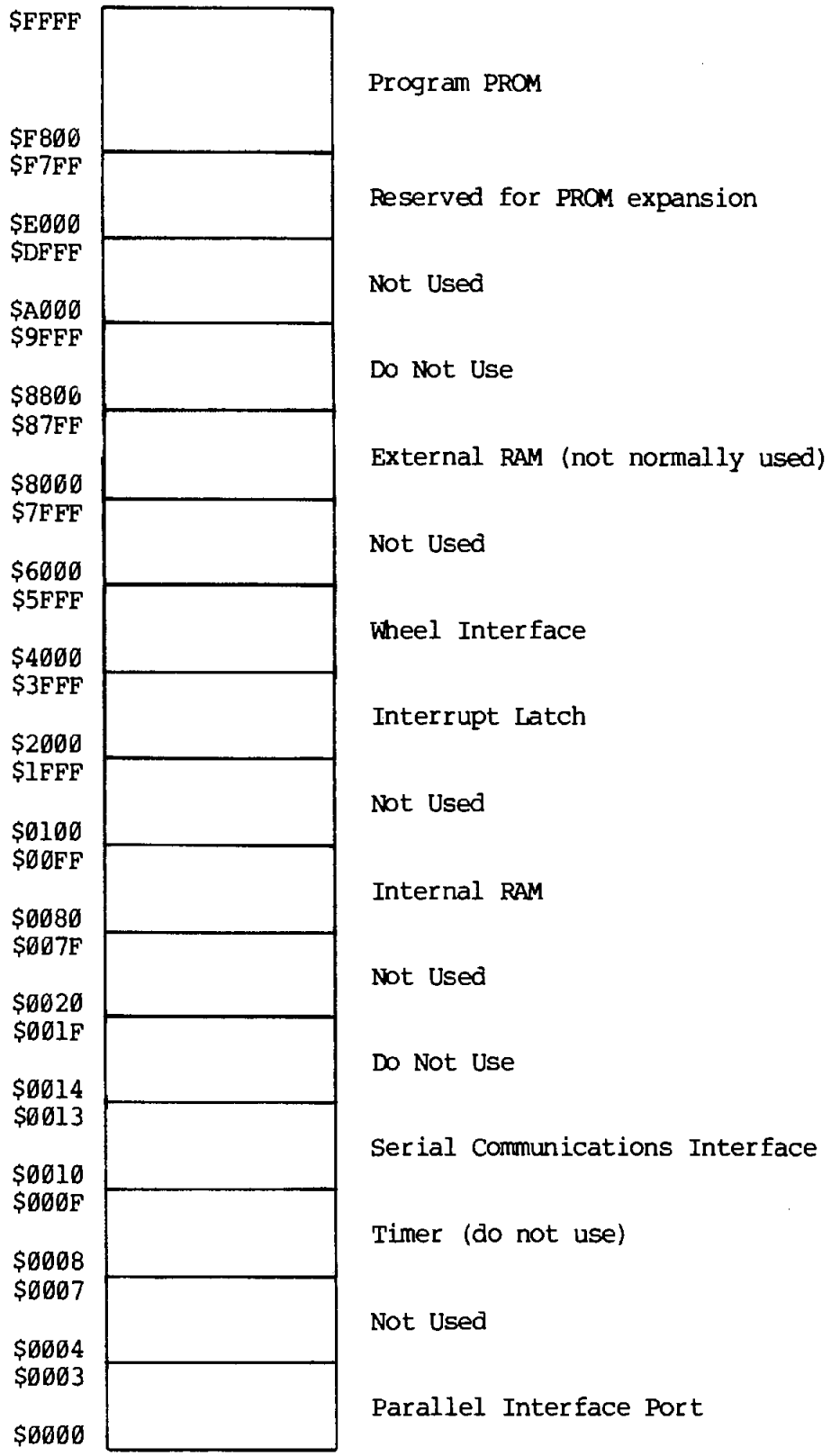
Addresses $8000 - $87FF are reserved for a 2Kbyte RAM (6116LP-4); this is not normally fitted.

iii) Wheel Interface

The channel control fader wheel is located at addresses $4000 - $5FFF; only address $4000 is normally used. When the MPU reads from this address the result is a twos complement value representing the direction and extent of wheel movement since the last read action.

iv) Interrupt Latch

The Panel Processor receives an Interrupt Request about every 1.5ms, from a latch which is set by a signal which enables the display drivers. When the MPU responds to this request, it resets the latch by writing to one of addresses $2000 - $3FFF; $2000 is normally used.



PANEL PROCESSOR ADDRESS MAP

Fig. 2.2.1

v) Internal RAM

Temporary data storage is provided by 128 bytes of random access memory (RAM) which forms part of the Panel Processor; the addresses used are $0080 - $00FF.

vi) Serial Communications Interface

The Panel Processor communicates with the Motherboard Processor via a serial link; this is controlled by a Serial Communications Interface, which forms part of the Panel Processor, and an Asynchronous Communications Interface Adapter (ACIA) on the Motherboard. Data is transmitted at 4800 baud and each data string consists of one Start bit, eight Data bits and one Stop bit. The Serial Communications Interface is located at addresses $0010 - $0013.

The communication protocol is described in section 2.2.4.

vii) Timer

The Panel Processor includes a programmable timer, located at addresses $0004 - $000F, which is not used in this application.

viii) Parallel Interface Port

The Panel Processor incorporates an 8-bit parallel interface port which is used to control the panel displays and indicators, and to detect button actions. Two matrices, one formed by the displays and indicators and the other by the buttons, are scanned simultaneously, about once every 12ms. The port registers are accessible via addresses $0000 - $0003.

2.2.2.2 Panel Processor Program

The Panel Processor program consists primarily of interrupt routines, the interrupt requests being generated by the Serial Communications Interface and the Interrupt Latch. On completion of

2.2.3 Motherboard and Executive Processor

The Motherboard is fitted behind the Panel Board and its processor (M68B09) controls the overall operation of the M24 system. The board includes the Tape Interface and communicates with the Panel Board and the Multiplex Interface units by means of serial links. Five multiway connectors allow additional, 'daughter' boards - in particular, the Video Interface - to be mounted directly onto the Motherboard.

2.2.3.1 Address Map

The Motherboard Processor address map is shown in Fig. 2.2.3 and described below:

i) Program PROM

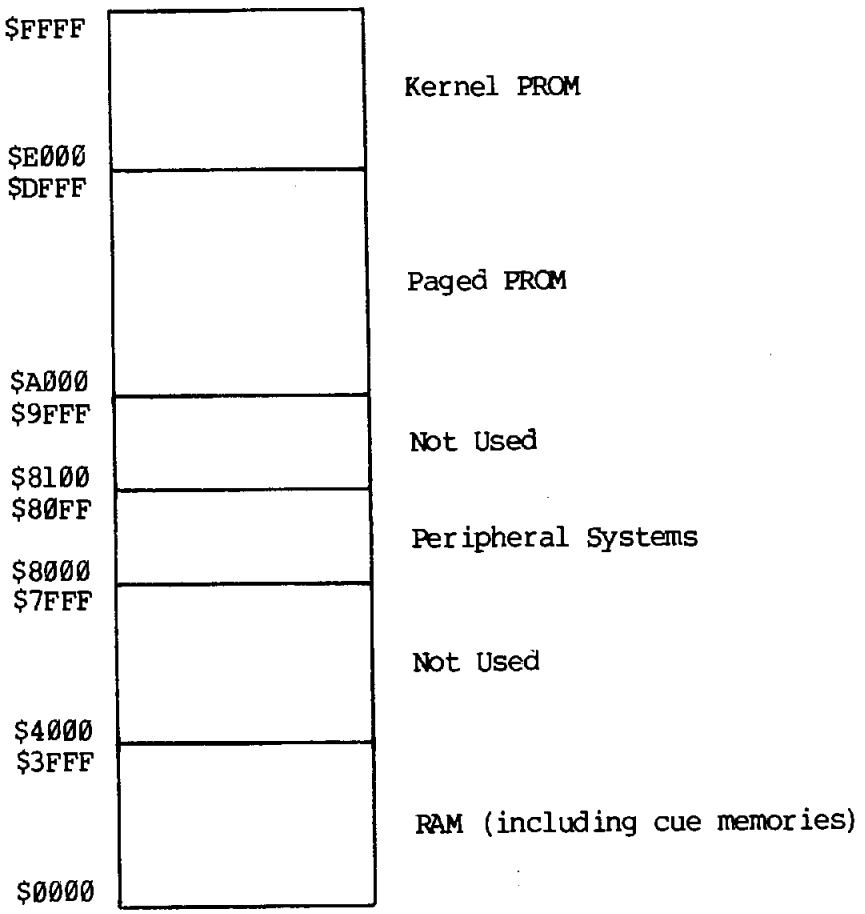
The Motherboard Processor program is held in U.V. erasable PROM (2764) located at addresses $A000 - $DFFF (Paged PROM) and $E000 - $FFFF (Kernel PROM). In the case of addresses $A000 - $DFFF, the PROM on the Motherboard is only one of eight 'pages' selected by a page register (part of the PIA). The other pages are not normally fitted, but if any optional facility requires additional program, the necessary PROMs are incorporated on the appropriate 'daughter' board.

ii) Peripheral Systems

Addresses $8000 - $80FF are reserved for the various peripheral systems as detailed in Fig. 2.2.4. Those located on the Motherboard have addresses in the range $8000-F, while the Video Interface (when fitted) occupies addresses $8010-B.

iii) Random Access Memory

The RAM located at addresses $0000 - $3FFF provides not only temporary storage for the Motherboard Processor, but also the lighting cue memories. Because of this, it is provided with a battery-maintained supply and may be protected by means of a



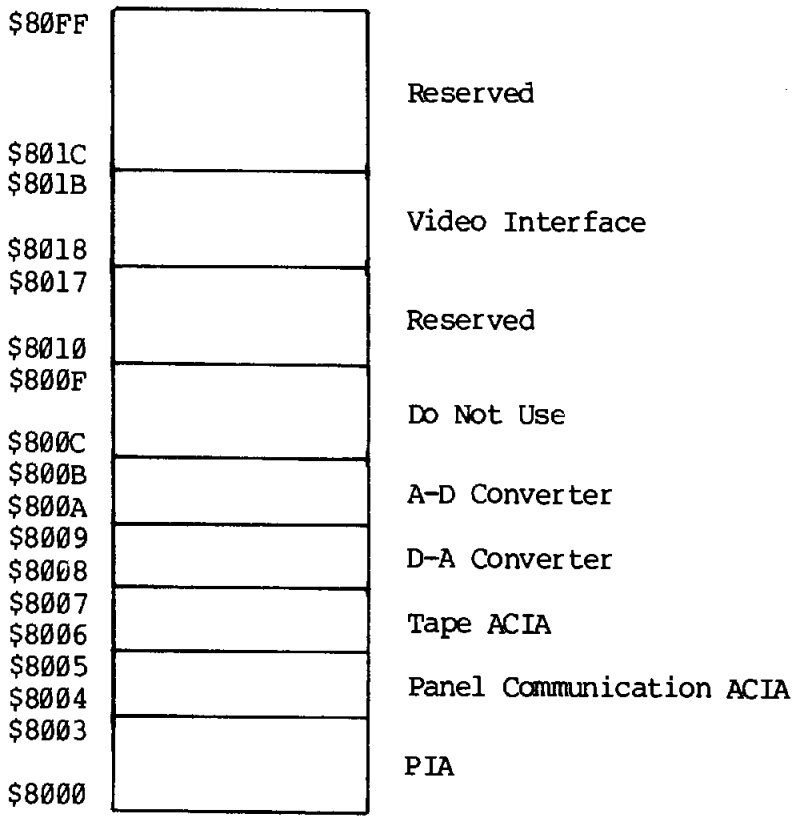
MOTHERBOARD PROCESSOR ADDRESS MAP

Fig. 2.2.3

memory lock system with a variable threshold. The lock is controlled by the REC LOCK keyswitch on the control panel and the threshold is set so that only the cue memories are protected.

2.2.3.2 Panel Communication Interface

The Motherboard Processor communicates with the Panel Processor by means of an Asynchronous Communications Interface Adapter (ACIA) at addresses $8004-5. The latter transmits and receives serial data at 4800 baud, the necessary clock signals being produced by a clock generator which also controls the Tape Interface. The data format is one Start bit, eight Data bits and one Stop bit, and the communication protocol is as described in section 2.2.4.



PERIPHERAL ADDRESS AREA

Fig. 2.2.4

2.2.3.3 Tape Interface

A second ACIA at addresses $8006-7 provides an interface with a cassette tape recorder the provision of which permits long-term storage of lighting cues. Data is transmitted and received in a CUTS format at 1200 baud. The transmission rate is determined by the clock generator mentioned in the previous section, while the receive clock signals are derived from the incoming data by means of an edge detector and a phase-locked-loop.

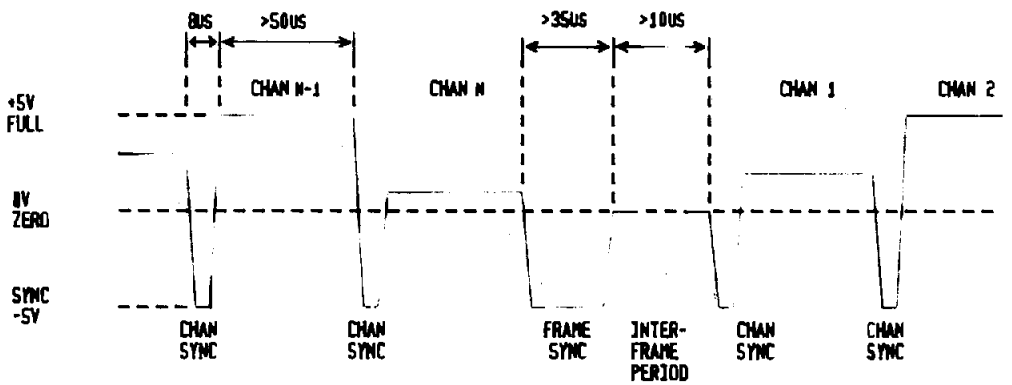
2.2.3.4 Analogue Interface

The Analogue Interface consists of a digital-to-analogue converter, which generates the multiplexed signal transmitted to the Multiplex Interface units, and an analogue-to-digital converter, which

receives the multiplexed 'Manual Fader Wing' signal from the Multiplexed Interface units and also the outputs from the four faders on the Panel board.

Two types of analogue output are possible: a two-wire system where the multiplexed analogue signal carries channel and frame sync pulses; and a four-wire system where the sync pulses are transmitted separately on a balanced line. In the latter case it is not possible to receive a multiplexed input from a manual fader wing.

Channel level data is written, in digital form, to a latch at addresses $8008-9 ($8008 is normally used). The latch outputs are applied to a digital-to-analogue converter and the analogue channel-level signal is routed to the output via a line driver circuit. The write action also triggers a monostable which produces a negative-going Channel Sync pulse; in the case of the two wire system, the latter overrides the analogue channel-level signal. At the end of each 'frame' of channels, a Frame Sync pulse is produced by the PIA. The form and timing of the two-wire multiplexed analogue signal is shown in Fig. 2.2.5; the four-wire signal is similar, but does not have the negative-going sync pulses superimposed upon it, these being transmitted separately.



MULTIPLEXED ANALOGUE SIGNAL

FIG. 2.2.5

The incoming 'Manual Fader Wing' signal from the Multiplex Interface units is applied to an analogue data selector, the other inputs to which are the four fader outputs from the Panel board (see section 2.2.2). The select inputs to this data selector are produced by the PIA. The selected output is stored on a capacitor and this stored level is applied to an analogue-to-digital converter controlled by the Motherboard Processor. When the conversion process is started by the MPU, the data selector is inhibited to prevent any change in the stored level. The conversion then takes place automatically and 15us later the result is read by the MPU via addresses $800A or $800B ($800A is normally used).

2.2.3.5 Motherboard Processor Program

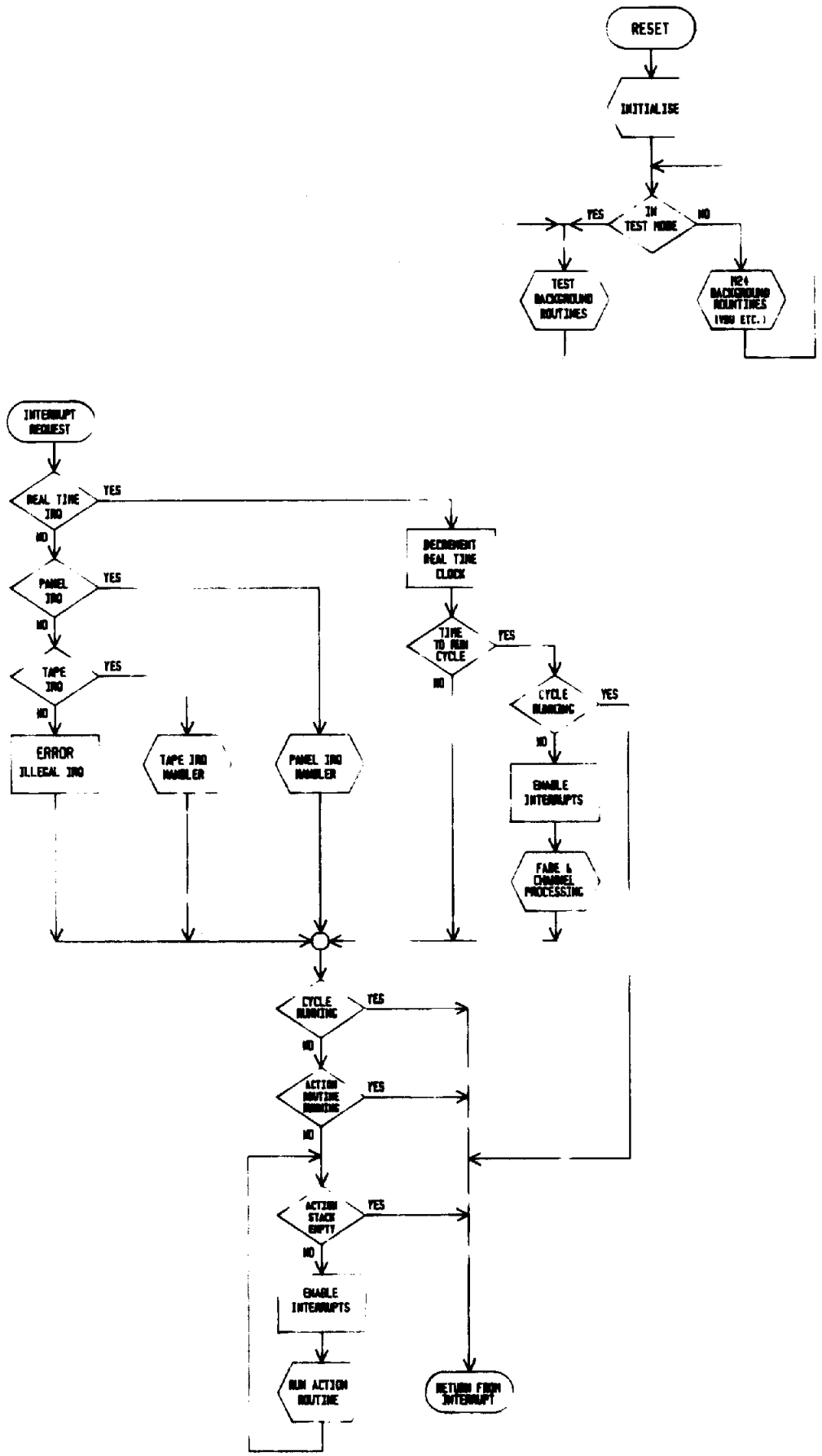
a) Power-up

On power-up, the Motherboard Processor first carries out the Power-up Self Tests and then initialises the RAM, ACIAs and PIA. It then reads the system configuration switches, enables interrupts and enters the background loop.

b) Background

When no other processing is being carried out, the Motherboard MPU runs in 'background'. Depending on the state of a flag, it will either run the 'Lighting System' background loop, or the 'System Tests' background loop.

The Lighting System background loop is responsible for updating the Video Mimic display and for some of the Tape routines. The System Tests background loop consults various flags which cause the various System Tests to start or stop. All the tests run at background level, and once System Test mode has been selected, it is not possible to return to normal mode without switching the system off.



MOTHERBOARD PROCESSOR PROGRAM

FIG. 2.2.6

c) Interrupts

When an interrupt request is received, the Motherboard Processor determines its source by polling the PIA and ACIAs. It then clears the interrupt flag and enters the appropriate interrupt routine.

Real-time interrupts cause an internal timer to be decremented; this timer controls the routines which deal with fade and channel processing, and with the preparation of mimic updates for transmission to the front panel. All these routines are run on a regular, cyclic basis.

Interrupts generated by the ACIAs cause the appropriate data transfer routines to be carried out. Action routines may also queued if appropriate.

When the interrupt handling is complete, the MPU checks to see whether 'cycle' processing or an Action routine was in progress when the interrupt occurred; if so, it returns to the interrupted routine. If not it checks the Action Stack; if this is empty it returns to background level. If, however, there are actions awaiting, interrupts are enabled and the required Action routines are then carried out, in turn, until the Action Stack is empty. The MPU then returns to background level.

2.2.4 Panel/Motherboard Communication

Communication between the Motherboard and the Panel board is by means of a serial link with a data transmission rate of 4800 Baud. The Serial Communications Interface in the Panel processor and the ACIA on the Motherboard are designed to operate independently of their respective processors and function by generating interrupt requests whenever they have received data or require data for transmission.

2.2.4.1 Communication Format

Data is normally transmitted as Address/Data two byte messages. The Address byte is transmitted first and identifies the button, etc. or display (depending on the direction of transfer) to which the following Data byte refers. Address bytes may have values from $00 to $FD, while the values $FE and $FF have special meanings which are described below. Data bytes may have any value from $00 to $FF.

The Data byte code varies depending on the control with which it is associated, as follows:

i) Panel to Motherboard

Buttons and switches	-	$80 = On. $00 = Off.
Wheel	-	$80 to $7F (twos complement). Positive values represent upward movement and negative downward.

ii) Motherboard to Panel

Numeric Displays	-	BCD code (1 or 2 displays/byte).
Mimic Lamps, etc.	-	$00 to $FF, 1 bit/mimic.

2.2.4.2 Control Bytes

An Address byte with the value $FF indicates that the byte following should be interpreted as a Control byte rather than a Data byte. Control bytes may have values $00 to $0F, $FC, $FD and $FF.

The values $00 to $0F are used to select address areas (pages). Because Address bytes can have only 254 unique values, this is the maximum number of buttons/displays which can be identified by an Address/Data pair. The use of sixteen address areas expands the capacity of the system by sixteen times. This capability is not normally used on M24.

The remaining Control byte values have the following meanings:

$FC	-	Pause Transmission.
$FD	-	Continue Transmission.
$FF	-	Requests the current status of all buttons/ displays (as appropriate).

2.2.4.3 Sync Byte

In order to ensure that Address and Data bytes are correctly interpreted, the Panel and Motherboard communication systems are synchronised by means of Address byte $FE. This has no Data byte associated with it and is generated by the Motherboard Processor every 30ms (approx). Whenever the Panel receives this byte, it responds by transmitting the same value to the Motherboard, before the next Address/Data pair. If the Panel does not respond correctly, the Motherboard Processor will recognise that a Sync error has occurred.

If the Panel receive system is not synchronised with the Motherboard, the Sync byte will be interpreted as Data and the next byte, correctly, as an Address. The two systems will thus be re-synchronised. Similarly, if the Motherboard receive system is not in synchronism with the Panel, the two systems will be automatically re-synchronised when the Sync byte is transmitted.

To ensure that the displays remain correct and that the Motherboard is aware of all Panel button actions, etc., whenever a Sync error is detected the Motherboard transmits the Address/Data pair $FF, $FF (Request current status) and sends the correct state for all the displays.

2.2.5 Video Interface

The Video Interface is an optional addition to the M24 system and is carried on a small plug-in 'daughter' board. This connects directly to the Motherboard via any one of five 'system bus' connectors. External connections are made via a video connector panel fitted in the rear extrusion of the desk, which incorporates a small board

carrying a UHF (or, in some cases, VHF) modulator; the video mimic may therefore be provided by either a standard monochrome television or, for improved display quality, by a television monitor.

The video interface carries 2Kbytes of Video RAM, a Cathode Ray Tube Controller (CRTC) and a Character Generator. Data loaded into the Video RAM by the Motherboard Processor is retrieved on a cyclic basis by the CRTC and converted into the video signals required by the Video Mimic.

The CRTC (6545) is a programmable device which is initialised by the Motherboard Processor each time the system is powered-up. The screen format consists of 25 lines of 64 characters each, and each character is formed in a 7 x 5 dot matrix. The scan rate is adjusted to be compatible with 50Hz or 60Hz systems (625/525 line respectively) as required, at a basic dot rate of 9.84375MHz.

Each location in the Video RAM corresponds to a particular position on the VDU screen. The Motherboard Processor does not, however, have direct access to the Video RAM, but must load the address of the required screen location into a register in the CRTC. This 'update' address is multiplexed with the video scan addresses so that, as the scan takes place, update and scan addresses alternate. The Motherboard Processor then writes to the Video RAM via address $8019, the write action being delayed, if necessary, by means of MRDY (see glossary - chapter 1), until the update address location is next selected. The characters loaded into the RAM are in a modified form of upper-case ASCII code (see Table 2.2.1).

Only six bits are necessary to represent the character, the remaining two bits (bits 6 and 7) being used to define the character 'Attribute', as follows:

DB6	DB7	Attribute
0	0	Normal Character
1	0	Flashing Character
0	1	Inverse Video Character
1	1	Dim Character

Table 2.2.1

DB3 DB2 DB1 DB0 \ DB5 DB4	Ø Ø	Ø 1	1 Ø	1 1
Ø Ø Ø Ø	@	P	(Space)	Ø
Ø Ø Ø 1	A	Q	!	1
Ø Ø 1 Ø	B	R	"	2
Ø Ø 1 1	C	S	#	3
Ø 1 Ø Ø	D	T	$	4
Ø 1 Ø 1	E	U	%	5
Ø 1 1 Ø	F	V	&	6
Ø 1 1 1	G	W	'	7
1 Ø Ø Ø	H	X	(	8
1 Ø Ø 1	I	Y	)	9
1 Ø 1 Ø	J	Z	*	:
1 Ø 1 1	K	[	+	;
1 1 Ø Ø	L	\	,	<
1 1 Ø 1	M	]	-	=
1 1 1 Ø	N	^	.	>
1 1 1 1	O	_	/	?

As each character is retrieved from the Video RAM by the CRTC, it is applied to a Character Generator integrated circuit, which produces dot signals. These, when displayed on the VDU screen, form the character concerned. The dots are converted to serial form, given the correct attribute and incorporated in a composite video waveform which is applied to the monitor.

The Video Interface is located at addresses $8018 - $801B in the Motherboard Processor address map.

2.3 MULTIPLEX INTERFACE UNIT

Each Multiplex Interface unit contains a single Multiplex/Demultiplex board which generates the dimmer drive outputs for 24 lighting channels and receives control inputs from the corresponding channels on the Manual Fader Wing. Each unit is self-contained and independently powered.

Where several Multiplex Interface units are provided these link together via 3-pin XLR connectors; only one connection is therefore necessary from the Control Console. The Manual Fader Wing inputs and dimmer drive outputs are either via 8-pin 'Bleecon' connectors or 25-pin miniature D-type connectors.

2.3.1 Channel Demultiplexer

The channel demultiplexer is responsible for sampling the incoming analogue multiplex signal from the Control Console and routing the appropriate lighting channel levels to the dimmer drive outputs.

The analogue multiplex signal takes the form shown in Fig. 2.2.5. The lighting channels levels are transmitted serially in numeric order, one complete transmission (frame) of all the channels controlled by the system occurring about every 5Øms. At the end of each frame, a channel counter is loaded with a preset value which depends on the group of channels served by the board, i.e. on the setting of the Channel Group Selector below the multiplex connectors. When the next frame begins, the Channel Sync pulses clock the counter and, when a particular counter state is established, the board is enabled. This state is the same for all the Multiplex Interface units, but because of the different preset values it occurs at a different time in the frame in each unit. Each unit is therefore enabled only when the levels of the channels it serves are being received.

During the period when the board is enabled, the analogue level is sampled and routed to the appropriate output circuit where it is stored on a capacitor. The required output is selected by the counter.

2.3.2 Channel Multiplexer

The Multiplex/Demultiplex board also includes a multiplexer which receives its inputs from the channel control outputs of the Manual Fader Wing. These inputs are selected by the counter in the same way as for the demultiplexer. The multiplexed signal is routed to the Control Console via a line driver circuit.

2.3.3 Independent Operation

The unit includes an oscillator which, in the absence of an analogue multiplex signal from the control console, permits the control signals from the Manual Fader Wing to be routed via the multiplexer and the demultiplexer to the dimmer drive outputs. This permits the Manual Fader Wing to be used if the M24 Control Console is inoperative.

2.4 M24Fx PATCH/EFFECTS UNIT

The M24Fx console contains one main printed circuit board (the Effects Processor board) and one smaller board, which forms part of the Power Supply unit.

2.4.1 Power Supplies

The low voltage supplies for the M24Fx electronics are taken from a single unit mounted in the base of the console. This unit has outputs at +15V, +5V and -15V and these are connected to the Effects Processor board as shown in Drawing No. 7C28189.

2.4.2 Effects Processor Board

This board is mounted on the rear of the control panel and carries the push-buttons, switches, faders and displays. Its microprocessor (M68B09) is responsible for the overall operation of the Patch system and also for generating the Chaser outputs for the Effects system. With the exception of the Chaser, the Effects are not microprocessor controlled, but are provided by dedicated circuits comprising a Flash Generator, a Sound-to-light Generator and momentary Flash buttons.

The board also includes a sync detector/generator by means of which the unit may act as a back-up to the M24 Console.

2.4.2.1 Address Map

The Effects Processor address map is shown in Fig. 2.4.1 and described below:

i) Program PROM

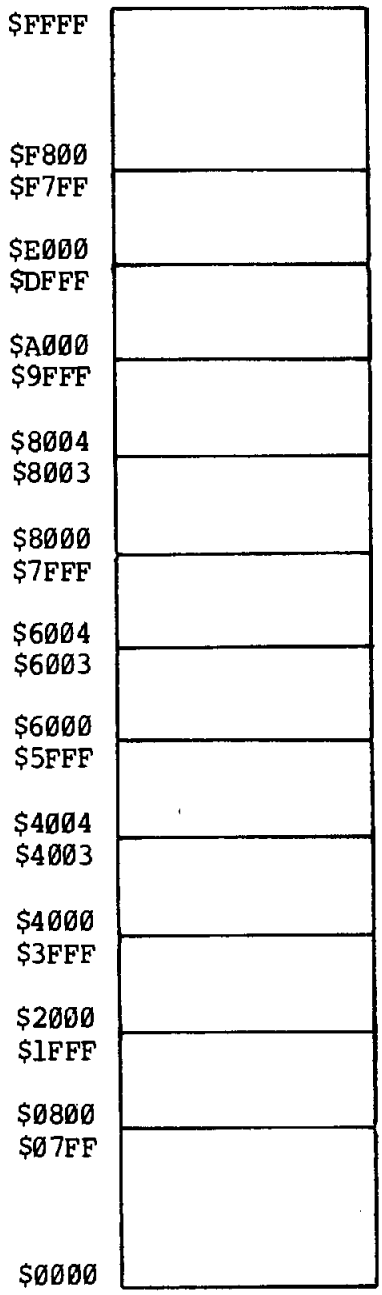
The Effects Processor program is held in ultra-violet erasable PROM (normally 2716) located at addresses $F800 - $FFFF. Note that addresses $E000 - $F7FF are reserved for future expansion.

ii) Alpha-numeric Display

A four-digit latching alpha-numeric display (keypad display) is located at addresses $8000 - $9FFF. This device is write-only and only if fact occupies four addresses, one for each digit; $8000-3 are normally used.

iii) Peripheral Interface Adapters

Two Peripheral Interface Adapters (PIAs) are provided at addresses $4000 - $5FFF and $6000 - $7FFF respectively. The first of these is used to scan the panel push-buttons and indicators and to generate real-time interrupts, while the



EFFECTS PROCESSOR ADDRESS MAP

Fig. 2.4.1

other provides the channel on/off and Chaser outputs. Other lines on both devices are used in connection with the sync detector/generator.

As in the case of the Alpha-numeric Display, the PIAs only occupy four addresses each, $4000-3 and $6000-3 being normally used.

iv) Random Access Memory

The RAM located at addresses $0000 - $07FF provides not only temporary storage for the Effects Processor, but also the Patch memories. Because of this, it is provided with a battery-maintained supply.

2.4.2.2 Patch Master Faders

The outputs from each Patch Master fader is routed via the OFF contact of the appropriate OFF/CHASE/FLASH switch to an analogue switch controlled by the Port B outputs of PIA 2. As each channel is scanned, the On/Off states for that channel in the eight patch memories are retrieved from the RAM and determine whether the combination of the master fader and the effects should appear at the output.

The eight Patch Master outputs and the multiplexed Manual Fader Wing signal from the Multiplex Interface units are combined together in a Highest-takes-precedence circuit and routed via a line driver circuit to the M24 Console.

2.4.2.3 Effects System

The automatic effects system comprises a Chaser, a Flash Generator and a Sound-to-light Generator. In addition, a momentary action Flash switch is associated with each of the Patch Master faders.

i) Chaser

The chase signals are generated by the MPU in response to interrupts produced, via PIA 2, by an adjustable rate pulse generator. The chase outputs appear on Port B of PIA 2 and these control eight analogue switches. Each of the latter routes the output of the EFFECTS MASTER to the CHASE contact of the corresponding OFF/CHASE/FLASH switch.

ii) Flash Generator

This consists of an adjustable slope saw-tooth generator, the output of which is compared with the setting of the MARK-SPACE control. There are two comparators, producing non-inverted and inverted flash signals for effects channels A, C and E, and B and F respectively.

iii) Sound-to-light Generator

The Sound-to-light Generator consists of an AGC circuit feeding three filters, bass, middle and treble. The output of each filter switches the EFFECTS MASTER output onto the appropriate contact of the corresponding OFF/CHASE/FLASH switch (Patch Masters F, G and H respectively).

The input to the Sound-to-light Generator may be taken from either channel (left or right) of a stereo signal connected via the DIN socket on the control panel. The system is intended to be driven from the pre-amplifier stage of a tape recorder, etc., and the input must not, under any circumstances, exceed 5V peak-to-peak.

As an alternative to the audio input, the Sound-to-light Generator may be driven from a Random Flicker Generator (position F on the L/R/F switch). This consists of four oscillators operating at different frequencies, the outputs of which interact to produce a pseudo-random output.

2.4.2.4 Sync Detector

In addition to providing patch and effects facilities, etc. M24Fx can act as a back-up to M24, thus permitting continued operation in the unlikely event of failure of the main console.

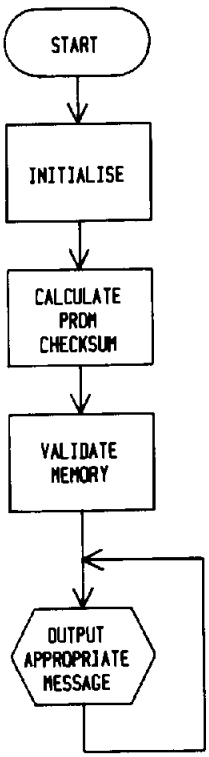
In normal operation, the multiplexed Manual Fader Wing signals from the Multiplex Interface units are combined on a highest-takes-precedence basis with the output of M24Fx and routed to the M24 Console, while the output from the M24 Console is routed to the Multiplex Interface units via M24Fx without additional processing. The timing of the operation is controlled by the sync pulses from M24.

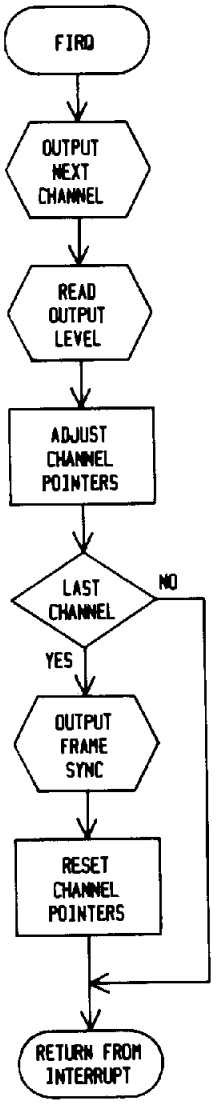
If for any reason the sync pulses from the M24 Console cease, a relay will change over, routing the combined Manual Fader Wing and M24Fx signals to the Multiplex Interface units, and M24Fx will generate sync pulses. These sync pulses will be superimposed on the multiplexed analogue output or transmitted separately, depending on whether the system in use is two-wire or four-wire.

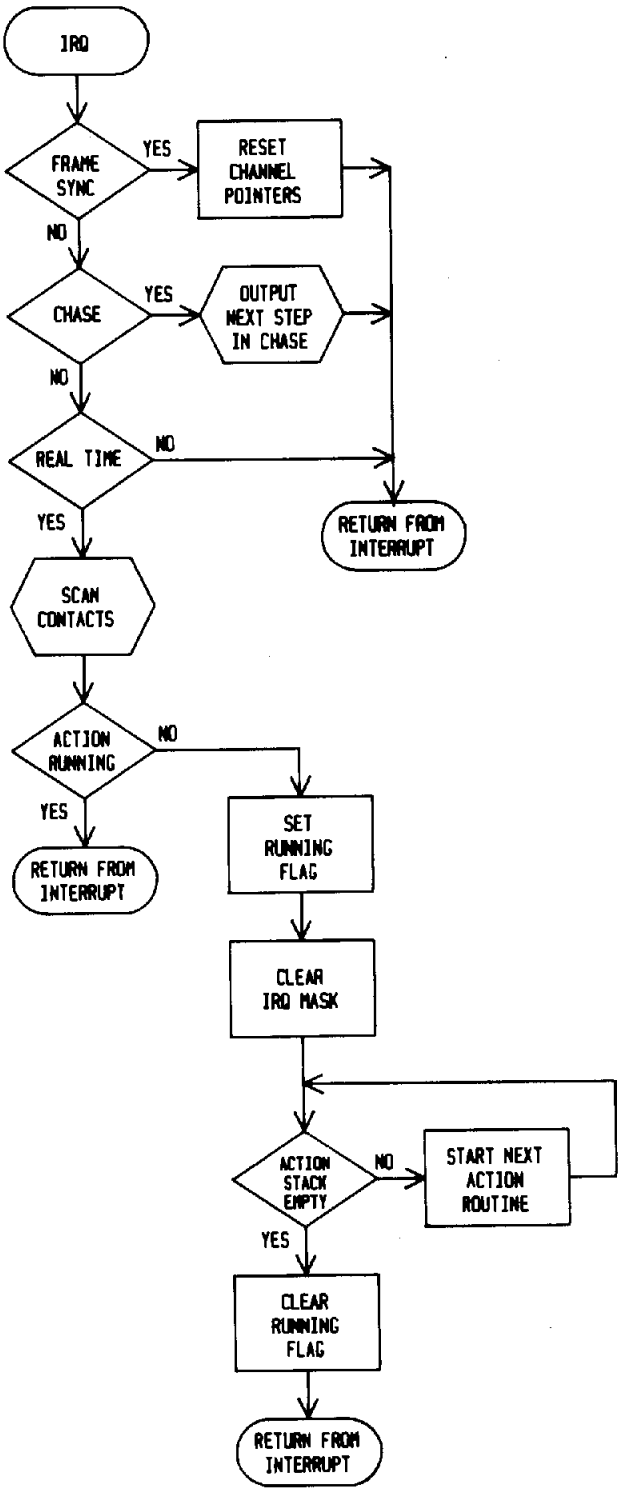
2.4.2.5 Effects Processor Program

The Effects processor program consists mainly of interrupt and action routines. Interrupt requests are generated by the two PIAs in response to multiplex sync pulses, the M24 Frame Sync signal, the Chase pulse generator output and Real Time Interrupt signals. Action routines are initiated in response to panel button operations and are added to an Action Stack for processing between interrupts.

On power-up, the system is initialised and the PROM checksum and RAM validation routines carried out. The MPU then enters the background loop to output the appropriate message.







EFFECTS PROCESSOR PROGRAM

FIG. 2.4.2

The interrupt routines are as follows:

i) Multiplex Sync Pulses

In order to ensure that channel levels are output at the correct rate, these interrupts are generated via the Fast Interrupt Request (FIRQ) input of the MPU.

On receipt of a FIRQ, the MPU outputs the on/off states of the next channel and, if necessary, reads the current overall output for use in the LOAD OUTPUT action routine. The channel pointers are then adjusted and, if the channel is the last one in the frame (i.e. channel 6Ø), the MPU outputs a Local Frame Sync signal and resets the channel pointers before returning to background or action level.

ii) Frame Sync Pulse

On receipt of a frame sync IRQ, the MPU carries out a routine to reset the channel pointers.

iii) Chase IRQ

When an IRQ is received from the Chase pulse generator, a routine to output the next step in the chase is carried out.

iv) Real Time IRQ

On receipt of a Real Time IRQ, the MPU scans the contacts and displays and, if appropriate, adds any new routines to the Action Stack for processing at action level. If an action routine is in progress, the MPU then returns to action level. If not, the Action Running flag is set and the IRQ Mask cleared, prior to testing the Action Stack; if this is empty, the Action Running Flag is cleared and the MPU returns to background level, but if not the MPU jumps to the next routine on the stack.

CHAPTER 3

CONTROL PANEL BOARD (Ref.1833)

Drawing No. 6A26904

3.1 INTRODUCTION

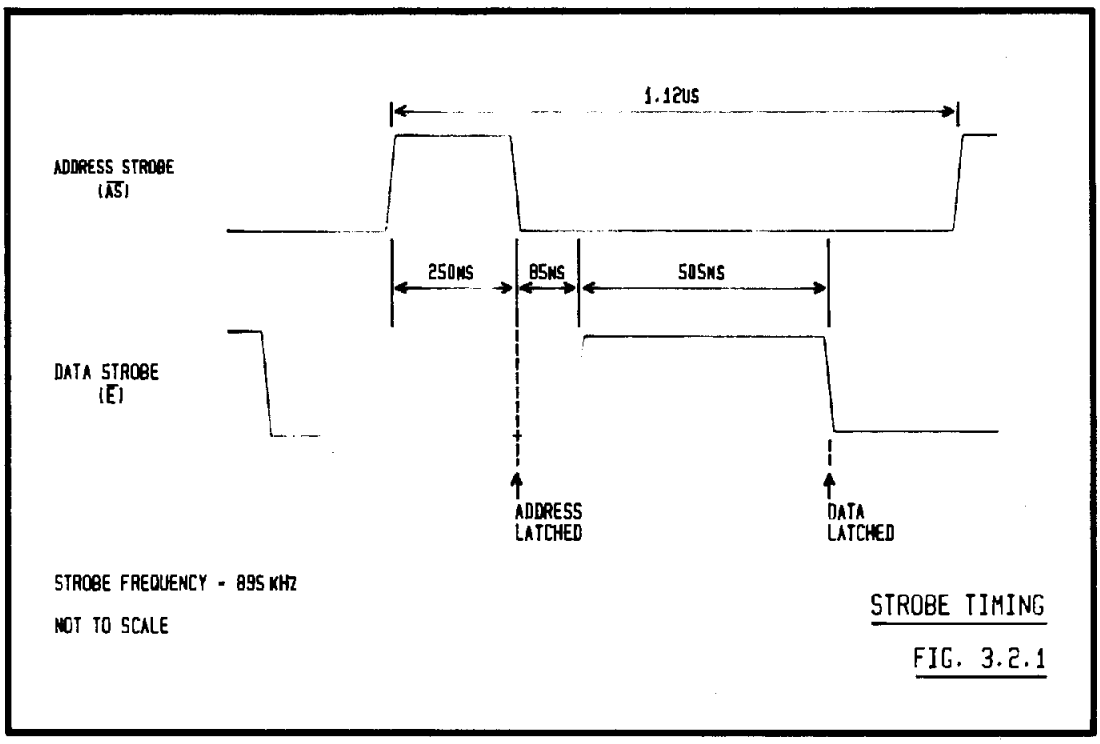
This board is mounted immediately behind the M24 control panel and carries the panel push-buttons and displays, and the Master Faders and Fade Duration controls. The board connects to the Motherboard via a 20-way ribbon cable.

In addition to the panel controls and displays, the board carries a microprocessor (Panel MPU) and a 2Kbyte PROM. The MPU scans the button contacts and the displays and communicates with the Motherboard Processor via a serial link.

3.2 THE MICROPROCESSOR

The Panel MPU, IC11, is a Motorola MC6803 8-bit microcomputer. It incorporates an 8-bit parallel interface port, which is used to scan the push-buttons and the displays, and a serial communications interface, which provides the link with the Motherboard Processor. In addition, the MPU includes a programmable timer, which is not used, and 128 bytes of random access memory (RAM).

Communication with the PROM and the channel control wheel is is by means of an eight-bit address bus (A8 - A15) and a multiplexed Data/Address Bus (D0/A0 - D7/A7). An Address Strobe ('AS') pulse generated by the MPU permits the separation of the address signals (in latch IC12), to produce address lines A0 - A7. This gives a total available address space (including those addresses internal to the microprocessor, i.e. RAM, etc.) of 64Kbytes ($0000 - $FFFF). Correct data timing is ensured by a Data Strobe pulse ('E').



STROBE TIMING

FIG. 3.2.1

The MPU derives the strobe signals from a 3.57945MHz crystal, XL, the output of which is divided by four to give a strobe frequency of 895kHz. The timing of the 'AS' and 'E' signals is shown in Fig. 3.2.1.

3.3 PANEL PROCESSOR ADDRESSES

Address lines A13 - A15 are decoded by IC7 to produce enable signals for the Program PROM ($E000 - $FFFF), External RAM ($8000 - $9FFF), Wheel Interface ($4000 - $5FFF) and Interrupt Latch ($2000 - $3FFF). Note that the addresses between $0000 and $00FF are assigned to locations within the MPU, the address bus being internally decoded.

3.3.1 Program PROM

The Program PROM, IC14, is a type 2716 2Kbyte EPROM located at addresses $F800 to $FFFF. The device is selected by a low output from pin 9 of decoder IC7 when A13 - A15 are all high, and its output is enabled by the low output of NAND gate IC8/12 when R/W and 'E' are both high.

It should be noted that the printed circuit board has been designed to allow an 8Kbyte PROM (type 2764) to be fitted and that the pin numbers shown on the circuit diagram apply to this device. The 2716 PROM is fitted with pin 1 in pin 3 of the dual-in-line socket.

3.3.2 External RAM

Provision is made for a type 6116LP-4 2Kbyte RAM (IC13) at addresses $8000 - $87FF. The device is selected by a low output from pin 5 of decoder IC7 and, for MPU read actions, its outputs are enabled by the output of NAND gate IC8/12 (see previous section). For write actions, a Write Enable pulse is produced by NAND gate IC8/6, which is enabled by 'E' and inverted R/W, except during Reset. IC13 is not normally fitted.

3.3.3 Wheel Interface

A fourteen pin DIL socket, SK1, is provided for connection to the channel control fader wheel. The movement of the wheel may be read via addresses $4000 -$5FFF ($4000 is normally used). When this takes place, a strobe pulse (STB) is generated by gating 'E' with the inverted output from pin 3 of IC7 in NAND gate IC8/8.

3.3.4 Interrupt Latch

Monostable IC4/7 is used as a latch and its output is applied to the IRQ1 input (pin 5) of the MPU. The device is reset by a low output from pin 2 of IC7, generated when the MPU accesses any address in the range $2000 - $3FFF. Address $2000 is normally used.

3.3.5 Address Locations within the MPU

The Panel MPU incorporates 128 bytes of RAM (addresses $0080 - $00FF), a Serial Communications Interface ($0010 - $0013), a programmable Timer ($0004 - $000F) and an 8-bit parallel interface port ($0000 & $0002). The Timer is not used in this application and its associated registers must not be accessed by the user.

3.4 SERIAL COMMUNICATIONS INTERFACE

Addresses $0010 - $0013 provide access to a Serial Communications Interface which is used to transfer data to and from the Motherboard Processor. The Transmit output appears on MPU pin 12 (Port 2, bit 4) and is routed via buffer IC3/6 to pin 2 of connector PL1, while the Receive input is routed via PL1 pin 3 and buffer IC3/4 to pin 11 (Port 2, bit 3) of the MPU. The transmission rate is determined by a clock signal (Tx/Rx CLK) which is generated on the Motherboard and routed via PL1 pin 1 and buffer IC3/2 to pin 10 (Port 2, bit 2) of the MPU.

The four Serial Communications Interface addresses provide access to the following registers:

$0010	Rate and Mode Register (write only).
$0011	Control and Status Register.
$0012	Receive Data Register (read only).
$0013	Transmit Data Register (write only).

Note: The Serial Communications Interface port (Port 2) may also be used as a parallel interface and addresses $0001 and $0003 provide access to its associated Data and Data Direction registers. The Data Register ($0003) is not used in this application, but the Data Direction Register ($0001) is initialised so that lines 0 and 4 are outputs and lines 1 and 3 inputs.

3.5 DISPLAY AND PUSH-BUTTON MATRICES

The 8-bit parallel interface port (Port 1) is used to control the panel displays and indicators and to detect button actions. Each time the equipment is switched on, the individual lines of the port are programmed by the MPU so that bits 0-6 will function as outputs and bit 7 as an input. This is done by means of a Data Direction Register located at address $0000. The port itself is accessible to the MPU via a Data Register located at address $0002.

3.5.1 Display Matrix

The displays and indicators are wired as an eight-by-eight matrix. The rows are connected to a shift register, IC1, which receives data from Port 1, bit 6 and clock pulses from Port 1, bit 1. The outputs of IC1 are applied to darlington drivers (IC2/1Ø - IC2/16 and VT11) each of which provides the common return for one of the rows.

The columns of the display matrix are driven by PNP darlington transistors VT3 - VT1Ø, which are themselves controlled by the outputs of decoder IC5. The select inputs to the latter are from bits 3-5 of MPU Port 1 and the device is enabled by the output (DISP EN) of monostable IC4/9.

3.5.2 Button Matrix

The panel push-buttons are wired as an eight-by-five matrix. The rows are selected by the outputs of decoder IC9, the binary inputs to which are provided by a counter (IC1Ø), clocked by the same signal (MPU Port 1, bit 1) as shift register IC1.

The columns are scanned by means of data selector IC6, the select inputs to which are bits 3-5 from Port 1 of the MPU. The state of the selected button matrix column appears on pin 3 of IC6 and is applied to bit 7 of MPU Port 1. Each contact has an associated diode to prevent interaction between the rows and columns which could lead to false results when several buttons are operated at once.

Because the select inputs to IC6 are the same signals as are used to select the required column in the display matrix, selection of a column in the latter results in the simultaneous selection of the corresponding column in the button matrix. This makes it possible for the MPU to scan both matrices at the same time.

3.5.3 Display and Contact Scan

On completion of each display and contact scan, monostable IC4/9 is triggered by a positive-going output from Port 1, bit 2. The resulting 1.5ms pulse (DISP EN) enables the display drivers and, on its trailing edge, triggers monostable IC4/7. The inverted output (pin 7) of the latter device is applied to pin 5 (IRQ1) of the MPU, generating an interrupt request.

The output of IC4/7 is also fed back via R29 to timing capacitor C9. Once the device is triggered C9 cannot charge because of the low pin 7 output and the monostable will therefore never time-out. It thus functions as a flip-flop set by the back edge of DISP EN and reset (on pin 3) by a low output from pin 2 of IC7 (see section 3.3.4).

When the MPU responds to the interrupt request, it first writes to address $2ØØØ to reset IC4/7 and then enters a routine to read one column of the button matrix and set-up the corresponding column of the display.

At the start of the scan, the required column in the two matrices is selected by means of MPU Port 1, bits 3-5 and counter IC1Ø is reset by a high output on bit Ø. At the same time, data for the first row of the display matrix is output on bit 6.

Bit Ø of Port 1 is then set low, allowing IC1Ø to count, and bit 1 is set high. The latter acts as a clock pulse to IC1Ø, thus selecting the first row of the button matrix, and also shifts the data on bit 6 into shift register IC1. The state of the selected contact is now read via bit 7 and, when this has been done and the information stored in the RAM, bit 1 is set low, ready for the next clock pulse. The data for the next row of the display matrix is then output on bit 6 and the process is repeated until all eight rows have been scanned.

On completion of the above, shift register IC1 will contain the on/off states for all the display segments and indicators in the selected column of the display matrix. The MPU now sets bit 2 of

Port 1 high and this triggers monostable IC4/9. The latter device produces a 1.5ms DISP EN pulse which enables decoder IC5, thus switching on the transistor (VT3 - VT1Ø) which drives the selected display column.

When IC4/9 has been triggered, the MPU returns to its normal processing, but at the end of the DISP EN pulse, it is again interrupted and the next column is scanned. The sequence repeats continually for each column in turn, so that each button contact is scanned about every 12ms and each display column is enabled for 1.5ms of this time. The frequency of this is such that the displays appear to be constantly illuminated.

3.6 MASTER FADERS AND FADE DURATION CONTROLS

The Master Faders and Fade Duration controls are mounted on the Control Panel Board, but are connected directly to the Motherboard via connector PL1.

3.7 RESET CIRCUIT

The reset circuit is formed by transistors VT1 and VT2, and their associated components. The circuit has two functions: firstly, to generate a reset pulse each time the equipment is switched on, thus ensuring that the MPU enters its start-up procedure correctly, and secondly, to inhibit processor operation if the voltage on the +5V rail varies by more than the allowed tolerance.

As the +5V rail (routed from the Motherboard via connector PL1) becomes established at switch on, VT2 will initially switch on because of the potential divider action of R7, R2, R3 and R11. This pulls the Reset line low. When the rail reaches +3.9V, zener diode D2 conducts and the voltage on the base of VT1 starts to rise until, with about +4.5V on the rail, this transistor switches on. VT2 is thus switched off and C1 begins to charge via R4. The Reset line will therefore rise with a time constant C1/R4.

If the +5V rail falls below +4.5V, VT1 turns off. This turns on VT2, clamping the Reset line to ØV. Also, the MPU may be reset by means of a manual reset switch, SW1.

In order to ensure correct MPU operation, three of the Port 2 lines must be held in the correct states during Reset. In addition to the RST pin (MPU pin 6) therefore, the Reset signal is connected via diodes to bits Ø and 2 of Port 2 (pins 8 and 1Ø) and bit 1 (pin 9) is connected via a resistor to +5V.

The Reset signal is also applied to NAND gate IC8/6, to prevent write pulses to the External RAM, and to monostable IC4/9, to inhibit the displays and indicators.

CHAPTER 4

WHEEL INTERFACE BOARD (Ref. 1706)

Drawing No. 6B24310

4.1 INTRODUCTION

This board converts the movement of the fader wheel into a form which can be read by a microprocessor. The wheel incorporates an inner disc with 212 slots which move past two photo-sensor devices as the wheel is operated. The extent of the movement is determined by counting the number of slots which pass the sensors and the direction by the phase relationship of the signals from the two sensors. This information appears on the outputs of an eight-bit latch in response to a strobe signal generated by the micro-processor. When the latch contents are read, the count is reset to zero, so that the output always represents the change in wheel position since the last read action.

4.2 MOVEMENT DETECTOR

The two photo-sensor devices, SEN1 and SEN2, each consist of an LED and a photo-transistor. Light generated by each LED is reflected from the surface of the disc and detected by the corresponding photo-transistor. The sensors and positioned so that the signals which they produce are 90° out of phase with each other as shown in Fig. 4.2.1.

The outputs from SEN1 and SEN2 are amplified by VT3 and VT2 respectively, and applied to input pins 4 and 13 of four-bit latch IC7. The latch is clocked by a 50kHz signal generated by an oscillator formed by IC5/2 and IC5/4, and their associated components.

The inverted outputs (pins 3 and 14) of these two latch bits are fed back to transistors VT3 and VT2 to assist the switch action, while the non-inverted outputs (pins 2 and 15) are applied to the

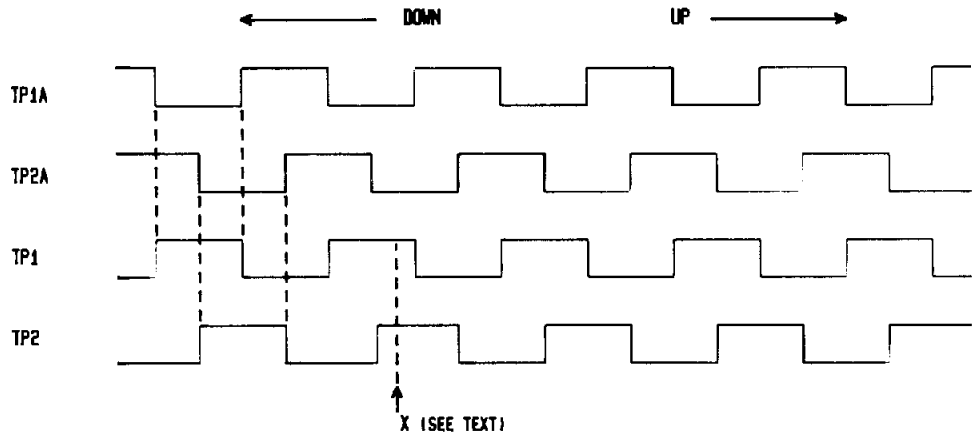


PHOTO-SENSOR WAVEFORMS

FIG. 4.2.1

remaining two latches on IC7 pins 5 and 12. As a result of the latter, any change detected by the photo-transistors will appear first on pin 2 or pin 15 (as appropriate) of IC7 and then, one clock cycle later, on pin 7 or pin 1Ø.

If there has been no change for the last two clock cycles, pins 2 and 7 will be in the same state and similarly pins 15 and 1Ø will be the same. A difference between the states of pins 2 and 7, or between pins 15 and 1Ø therefore indicates that the wheel has moved.

The four non-inverted outputs of IC7 are applied to the select inputs (A, B, C and D) of a 4-line-to-16-line decoder, IC6. The outputs of this device may be divided into three groups:

i) Those which appear for input states where A=C and B=D (binary Ø, 5, 1Ø and 15), or where both A and C, and B and D are different (binary 3, 6, 9 and 12). The first four will appear if the wheel is not moving and the others are invalid states.

ii) Those which appear if A or D are in a different state from the other three inputs (binary 1, 7, 8 and 14). These appear if the wheel is moved up.

iii) Those which appear if B or C are in a different state from the other three inputs (binary 2, 4, 11 and 13). These appear if the wheel is moved down.

The outputs in the first group (IC6 pins 9, 6, 4, 3, 22, 21, 19 and 16) are connected together as a Wired-OR (NO CH) and, after inversion, applied to the Carry-In input of a counter formed by IC4 and IC2. Similarly, those in the second group (IC6 pins 8, 2, 23 and 17) are connected together (DN) and applied to the Up/Down inputs of IC4 and IC2. The counter is clocked by the inverted output of the 50kHz oscillator and thus changes state on the opposite edge of the clock to latch IC7.

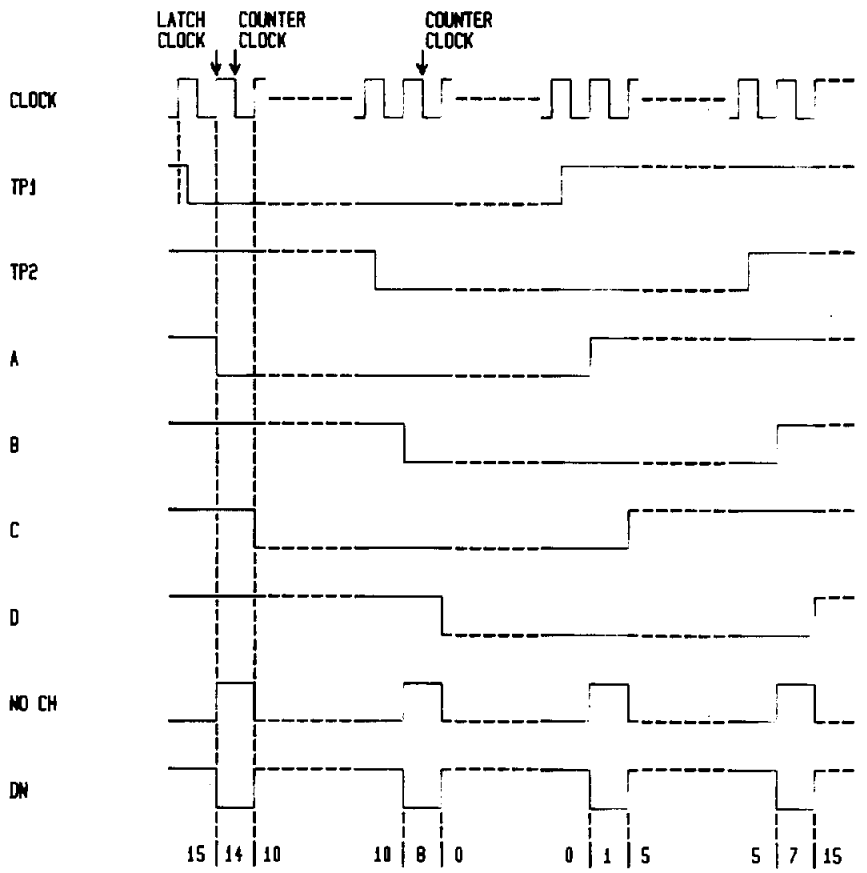
4.3 THE COUNT PROCESS

With the wheel stationary, the inputs to IC6 will be in one of the four valid states given in group 1 above; i.e. binary 0, 5, 10 or 15. Assuming, for the sake of illustration, that this state is binary 15 (as at 'X' in Fig. 4.2.1), moving the wheel upwards will cause TP1 to go low. On the next clock edge from IC5/4, therefore, decoder input A will be set low, thus producing a low DN signal. At the same time the NO CH signal goes high, enabling the counter. The count action occurs half a clock cycle later. Note that for upward movement of the wheel IC4 and IC2 count DOWN. The count process continues as the wheel is moved, as shown in Fig. 4.3.1.

When the wheel is moved downwards the process is similar, but in this case one of the unconnected outputs of IC6 is set low and no DN signal is produced. The counter therefore counts UP. The sequence of events is shown in Fig. 4.3.2.

4.4 COUNT LIMIT DETECTION

The most significant output of IC2 (pin 2) is applied to four exclusive OR gates: IC1/3, IC1/4, IC1/10 and IC1/11. The four next most significant counter outputs (IC2 pins 14, 11 and 6, and IC4 pin 2) respectively provide the second input to each of these gates. The outputs of the four gates are combined via diodes and, via IC5/12 and diode D5, connected to the NO CH line from IC6.



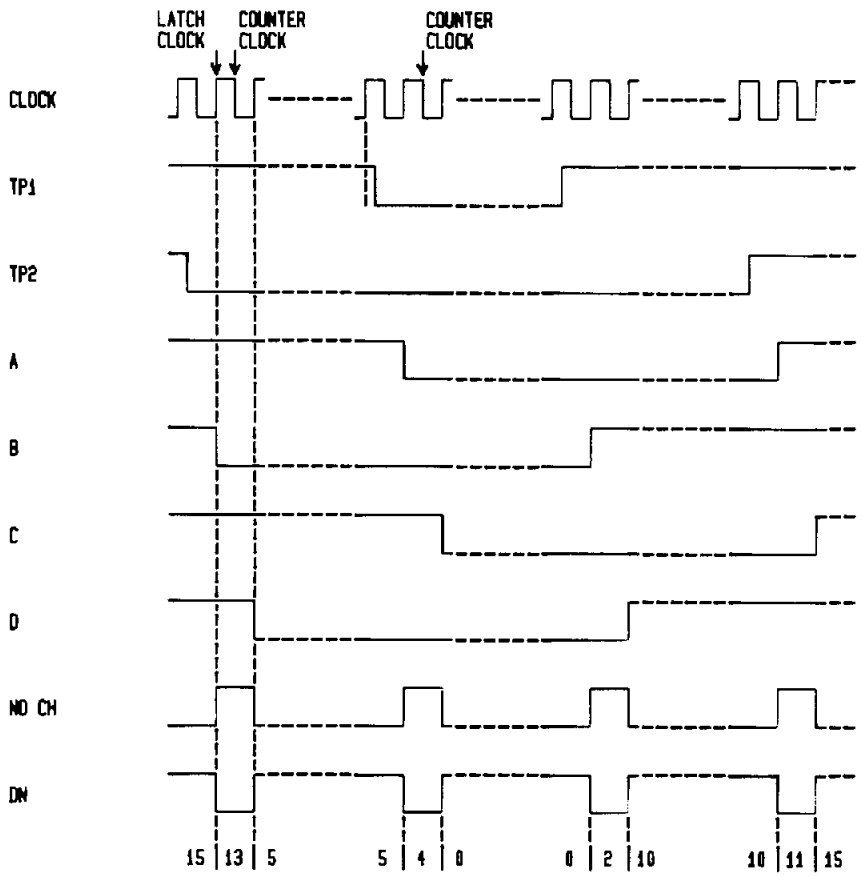
COUNT PROCESS - MOVE UP

FIG. 4.3.1

If the counter outputs reach a twos-complement value of +120 (01111000) or -120 (10000111), all four gates produce high outputs. The NO CH line is therefore pulled low via D5 and the counter is inhibited. This 'count limit' prevents the false readings which would result if the counter was allowed to overflow.

4.5 MICROPROCESSOR READ ACTION

The outputs of the counter provide the data inputs to an eight-bit latch, IC3. This device has two other inputs, on pins 11 and 1, which respectively latch the inputs from the counter and enable the three-state outputs. The latch signal is also applied, via VT1, to



COUNT PROCESS - MOVE DOWN

FIG. 4.3.2

the Preset Enable inputs of counters IC2 and IC4. Because the Preset inputs to the counters are connected via resistor R5 to +5V, they will be set to a twos-complement value of -1.

Although separate latch and output-enable inputs inputs are provided, the same signal is normally applied to both. A single negative-going pulse will then latch the counter outputs, enable the latch outputs and reset the counter.

CHAPTER 5

MOTHERBOARD (Ref. 1832)

Drawing No. 6A26932 (2 Sheets)

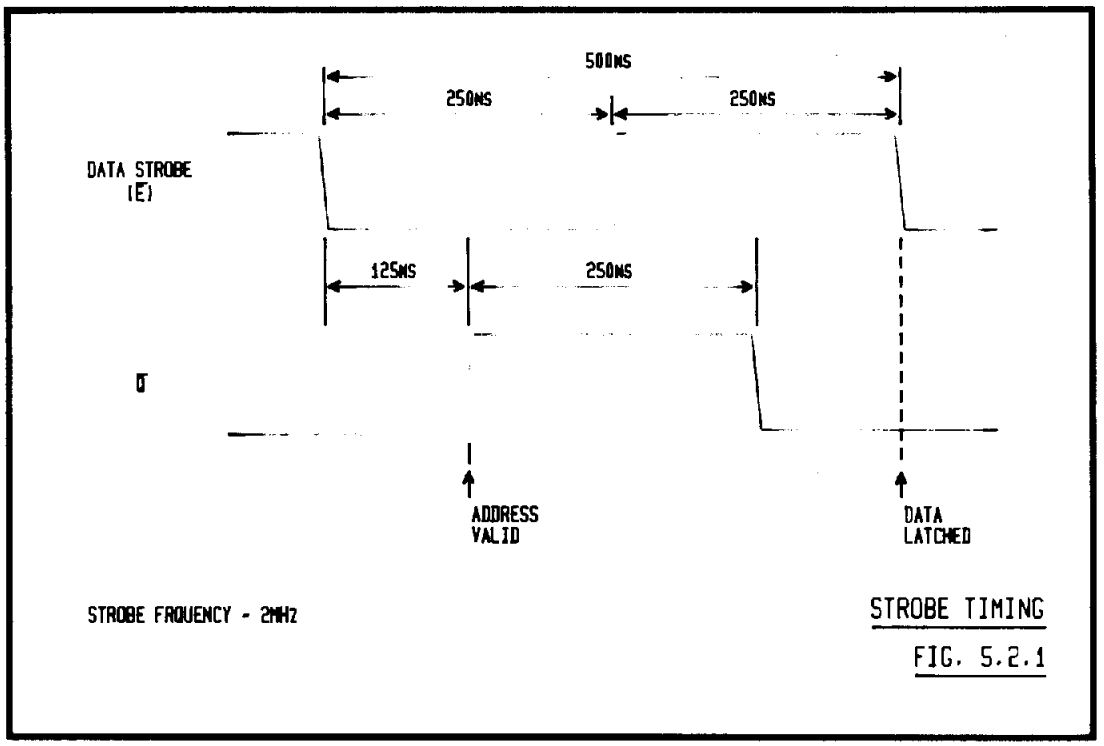
5.1 INTRODUCTION

The Motherboard controls the overall operation of the M24 system. It has five sockets for plug-in 'daughter' boards and communicates with the Control Panel board via a serial link.

The board carries a microprocessor (Motherboard MPU); a Peripheral Interface Adapter (PIA); an Asynchronous Communications Interface Adapter (ACIA) for communication with the Control Panel board; a second ACIA associated with a tape interface; a circuit which transmits serial channel level data to the Multiplex Interface units; and a multi-input Analogue-to-Digital converter which receives the multiplexed 'Manual Fader Wing' signal from the Multiplex Interface units, and also converts the analogue outputs of the control panel faders into digital form. The program is stored in three 8Kbyte EPROMs (2764-4) and eight 2Kbyte RAMs provide temporary and cue memory storage.

5.2 THE MICROPROCESSOR

The Motherboard MPU (IC23) is an MC68B09 8-bit micro-processor and this communicates with the rest of the system by means of an 8-bit Data Bus (D0 - D7) and a 16-bit Address Bus (A0 - A15). The total available address space is 64Kbytes ($0000 - $FFFF), but this is increased in practice by using a page register to select one of eight pairs of 8Kbyte PROMs at addresses $A000 - $DFFF. On the basic system, only one of these 16Kbyte pages is used, but where additional facilities are provided, paged PROMs are incorporated on the plug-in 'daughter' boards as necessary.



STROBE TIMING

FIG. 5.2.1

Correct data timing is ensured by strobe pulses 'E' and 'Q', which are derived by the MPU from an 8MHz crystal, XL2. The output of this is divided by four to give a strobe frequency of 2MHz. The timing of the 'E' and 'Q' signals is shown in Fig. 5.2.1.

5.3 MOTHERBOARD PROCESSOR ADDRESSES

Motherboard MPU address lines A13 - A15 are decoded by IC36 to produce enable signals for the Kernel PROM ($E000 - $FFFF), the paged PROMs ($A000 - $DFFF) and the battery-maintained RAM ($0000 - $3FFF). In addition, wired-AND circuits produce signals which select the peripheral systems ($8000 - $80FF) and, in particular, the on-board peripherals ($8000 - $800F).

5.3.1 Kernel PROM Addresses

The output from pin 9 ($E000 - $FFFF) of IC36 selects PROM IC22. The outputs of this device are enabled by NAND gate IC41/8, which receives 'E', R/W and LDATA. The latter signal is normally held high by a resistor (RN2), but may be set low to disable the Kernel PROM when using the Test Console (connected to the MC9 Test Port).

The signal from IC36 pin 9 is also used, via link LK5 and -NOR gate IC57/6, to trigger monostable IC46/4. This device produces a 400ns negative-going pulse which is routed via buffer IC11/8 to the MRDY input (pin 36) of the Motherboard MPU, IC23. This stretches the MPU cycle to allow for the slow EPROM devices. If a faster (200ns) PROM is fitted, the Kernel PROM MRDY signal may be disabled by cutting link LK5.

5.3.2 Paged PROM Addresses (Page 0)

The outputs from pins 6 and 7 of IC36 respectively enable PROMs IC29 ($A000 - $BFFF) and IC25 ($C000 - $DFFF). The outputs of the selected device are enabled by the output of inverter IC37/4, the input to which is from a wired-AND circuit which receives the inverted output of IC41/8 (see previous section) and the three Page Register outputs (PR0 - PR2) from the PIA (IC21). When the MPU is reading from a Paged PROM address, the wired-AND will only be fully enabled if all three Page Register outputs are low, i.e. if Page 0 is selected.

As in the case of the Kernel PROM, the Paged PROM chip select signals from IC36 are routed via -NOR gate IC57/6 to trigger monostable IC46/4 and thus generate a MRDY signal. If 200ns PROMs are fitted, links LK4 (IC25) and LK3 (IC29) may be cut to disable the MRDY signal.

5.3.3 RAM Addresses

The outputs from pins 1 and 2 of IC36 (addresses $0000 - $1FFF and $2000 - $3FFF respectively) are each used to enable one half of decoder IC53. The select inputs to this device are address lines A11 and A12 and its outputs are applied to the Chip Select inputs of the RAMs as follows:

IC53 pin	Address Range	RAM Selected
7	$0000 - $07FF	IC38
6	$0800 - $0FFF	IC42
5	$1000 - $17FF	IC48
4	$1800 - $1FFF	IC54
9	$2000 - $27FF	IC39
10	$2800 - $2FFF	IC43
11	$3000 - $37FF	IC49
12	$3800 - $3FFF	IC55

The outputs of the selected RAM are enabled, during read actions, by the output of NAND gate IC41/8, i.e. with R/W and 'E' both high - see section 5.3.1. During write actions, a Write Enable pulse is produced by NAND gate IC41/6. This gate is enabled by 'E', inverted R/W and a wired-AND circuit formed by transistors VT3 and VT13, and NAND gate IC41/12.

5.3.3.1 Memory Lock

In addition to the working stores required by the MPU, the RAMs provide the long-term memories in which lighting states are recorded. These may be protected against erasure by means of a keyswitch (REC LOCK) on the control panel and are retained when the system is not in use by a battery-maintained power supply.

When the REC LOCK keyswitch is in the 'locked' position, line PA7 (MLOCK) of the PIA (IC21) is set high and this partially enables NAND gate IC41/12. The second input to this gate is from binary comparator IC47. The latter compares a three bit 'lock-threshold', (PA0 - PA2) from lines PA3 - PA5 of the PIA, with address lines A10 - A13. A fourth lock-threshold bit (IC47 pin 1) is always low.

If the MPU writes to a RAM address where the binary value of A10 - A13 is less than or equal to that of the four lock-threshold bits, pin 5 of IC47 is low and IC41/12 is inhibited. IC41/6 is therefore enabled and the write action takes place regardless of the state of the MLOCK signal. If, however, the address is such that the value of A10 - A13 is greater than the lock-threshold, pin 5 of

IC47 is high, partially enabling IC41/12. If MLOCK is also high (memory locked), the latter gate is fully enabled and its low output inhibits IC41/6, thus preventing the write action.

The lock-threshold may be set by the MPU to any one of eight positions in the address map. The lowest position is at address $0400, so that the MPU will always have at least 1Kbyte of working RAM. A further 1Kbyte is added to this for each increase in threshold value, up to a maximum of 8Kbytes. The threshold is set by the MPU on power-up, its position depending on the number of channels controlled by the system.

5.3.3.2 Reset Write Inhibit

In order to ensure that the RAM cannot be corrupted during power-up and power-down, transistor VT3 pulls down pin 3 of IC41/6 during Reset, thus preventing the appearance of spurious Write Enable pulses. On power-up, a second transistor (VT13), controlled by line PA6 of the PIA, ensures that no RAM write actions take place until the lock-threshold has been established and the system fully initialised.

When the PIA is reset, all the lines of Port A are initially high, so that VT13 is switched on, thus pulling down the pin 3 input of IC41/6. This state will remain unchanged until the MPU has initialised the PIA, a process which includes the setting the correct lock-threshold.

5.3.3.3 RAM Bus Buffers

The RAM address and data signals are buffered from the rest of the Motherboard in order to minimise the risk of discharging the batteries too rapidly when the system is switched off or on.

The data lines from the MPU are routed to the RAMs via inverting bi-directional buffers IC33. These are enabled by the inverted output of -NAND gate IC40/11 whenever the MPU accesses one of the RAM addresses. For read actions, the low output from IC41/8 (see section 5.3.1) allows the buffers to drive the MPU bus, while for

write actions, IC41 pin 8 remains high and the buffers drive the RAM data inputs. When the system is unpowered, the RAM data lines are pulled low by resistors RN3.

The MPU address lines are also routed to the RAMs via buffers (IC32 and IC34). Note that 'E' and R/W are routed via IC34/9 and IC34/12 respectively. When the system is unpowered, the RAM address lines (A0 - A10) are pulled low by resistors RN5, while the Chip Select, Write Enable and Output Enable lines are pulled up to +VRAM (battery-maintained +5V).

5.3.3.4 Battery Circuit

The battery charging circuit is formed by VT11 and its associated resistors. With the system powered-up, VT11 is switched on and current flows from the +5V rail to power the RAMs and, via resistor R83, to charge the batteries. When the power is removed, VT11 is reverse biased and the batteries supply power to the RAMs via Schottky diode D24.

5.3.4 Peripheral Interface Addresses

All peripheral systems are allocated addresses in the range $8000 - $80FF. A 'Valid Peripheral Address' signal (VPA) is produced by gating together MPU address line A15 and inverted lines A8 - A14 in a wired-AND circuit formed by IC15, IC16/2 and IC11/3. This circuit may be inhibited by LDATA (via IC11/11) when using the 6809 Test Console.

Two further signals are derived from the Address Bus in order to select the area allocated to the on-board peripherals (PIA, ACIAs and A-D and D-A converters). A second wired-AND circuit, formed by IC16/6, IC16/10, IC16/4 and IC16/12, gates together inverted address lines A4 - A7, producing a signal ($xx00 - $xx0F) which is high whenever A4 - A7 are low. The latter signal is gated with VPA in NAND gate IC14/3, the output of which is low whenever the MPU accesses the on-board peripheral address locations.

The individual peripheral interfaces are selected by decoder IC31. This receives A1 and A2 on its select inputs and is divided into two sections. The first of these (1) is enabled by 'E' and the output of NAND gate IC40/8. The latter gate produces a low output when A3 is high and $8000 - $800F low. The second half (2) of IC31 is enabled when A3 is low.

The outputs from pins 9 and 10 (2-0 and 2-1) of IC31 are connected together and applied to the CS2 input of PIA IC21. Similarly the CS2 inputs of ACIAs IC28 and IC24 respectively receive the outputs from pins 11 (2-2) and 12 (2-3) of IC31. The PIA and ACIAs are all enabled (on their CS0 and CS1 inputs respectively) by $xx00 - $xx0F and VPA, so that the PIA is at addresses $8000-3, ACIA IC28 at $8004-5 and ACIA IC24 at $8006-7. The ACIA registers are selected by A0 and those in the PIA by A0 and A1.

There is no provision for additional chip select signal on the A-D and D-A circuits and the first half (1) of IC31 must therefore produce fully decoded signals with 'E' timing. For this reason the 'on-board peripherals' signal ($8000 - $800F) is gated with A3 in IC40/8 and applied to one enable input of IC31, and a second enable is provided by 'E'. The output from pin 7 of IC31 (addresses $8008-9) selects the D-A converter and that on pin 6 (addresses $800A-B) the A-D converter. Note that the latter signal is also routed via -NOR gate IC 57/6 to monostable IC46/4, thus generating a MRDY signal (see section 5.3.1).

5.4 SYSTEM BUS INTERFACE

The Motherboard carries five multiway sockets for the connection of plug-in 'daughter' boards, which are used to extend the facilities offered by the basic system. The additional electronics carried by these boards is accessible to the Motherboard MPU by means of a System Bus which carries all the MPU address and data lines, and the following control signals:

Signal	Input/Output	Buffer	Connector Pin
'E'	Output	IC10/18	17a
'Q'	Output	IC10/16	18a
R/W	Output	IC10/14	8c
VPA	Output	IC10/12	24c
156.3kHz clock	Output	IC10/3	19c
PR2	Output	IC10/5	27a
PR1	Output	IC10/7	27c
PR0	Output	IC10/9	26a
MRDY	Input	IC20/6	19a
FIRQ	Input	IC20/8	21a
IRQ	Input	IC20/10	21c
NMI	Input	IC20/12	20a
Reset	Output-Input	IC20/2-IC20/4	20c

Note: In the case of Reset, the signal generated on the Motherboard is routed to the MPU via the System Bus. This both ensures that devices on the daughter boards receive the Reset signal and allows the Motherboard MPU to be reset by a signal generated on a daughter board.

The Address Bus is routed via buffers IC18 (A0 - A7) and IC19 (A8 - A15), and the Data Bus via bi-directional buffers IC17. The latter are controlled by the output of -NOR gate IC56/8 which produces a high output, enabling the bus drivers, for all MPU write actions and for read actions at any of the on-board addresses. The signals concerned are as follows:

IC56/8 pin	Signal/Address	Function
6	R/W	All write actions
12	IC36 pin 1 ($0000 - $1FFF)	RAM
11	IC36 pin 2 ($2000 - $3FFF)	RAM
1	$8000 - $800F	On-board peripherals
2/3	IC40/6	Paged PROM - page 0
4/5	IC36 pin 9 ($E000 - $FFFF)	Kernel PROM

In the case of the Paged PROM signal, NAND gate IC4Ø/6 receives the output of a -NOR gate, IC4Ø/3, which in turn receives the pins 6 and 7 outputs of IC36 (addresses $AØØØ - $DFFF). IC4Ø/6 is only fully enabled, however, if its pin 5 input (from the wired-AND described in section 5.3.2) is high; i.e. if PROM Page Ø is selected.

The data buffers may be disabled by LDATA when the 68Ø9 Test Console is in use, but the address and control output buffers are always enabled. Note that all output signals are inverted on the bus.

5.5 PERIPHERAL INTERFACE ADAPTER

The peripheral lines of PIA IC21 are summarised in Table 5.5.1. The functions of most of the signals are described in the relevant sections of the text.

Table 5.5.1

PIA Line	Input/Output	Signal Title	Function
PAØ	Output	PRØ	PROM Page Select
PA1	Output	PR1	
PA2	Output	PR2	
PA3	Output	PAØ	RAM Lock Threshold
PA4	Output	PA1	
PA5	Output	PA2	
PA6	Output	Write Inh.	Power-up Memory Protect
PA7	Output	Mlock	Memory Lock
CA1	-	Not Used	-
CA2	Output	EOF	End of Frame pulse (see section 5.7)
PBØ	Input	-	System configuration switch inputs
PB1	Input	-	
PB2	Input	-	
PB3	Input	-	
PB4	Output	-	Configuration switch select
PB5	Output	PB5	Configuration switch and Analogue Input select.
PB6	Output	PB6	
PB7	Output	PB7	
CB1	Input	15ØHz	Real Time Clock
CB2	Output	Audio Test	Test Enable

The system configuration switches are scanned on power-up by means of outputs PB4 - PB7. There are four groups of four switches and the relevant group is selected by setting the corresponding output high. The switch settings may then be read via inputs PB0 - PB3. Note that outputs PB5 - PB7 are also applied to the Analogue-to-Digital converter circuit in order to select the required analogue input (see section 5.7).

5.6 PANEL COMMUNICATION INTERFACE

The Motherboard MPU communicates with the Panel MPU (see chapter 3) by means of an Asynchronous Communications Interface Adapter (ACIA), IC28. The information consists of serial data which is transmitted at 4800 baud via separate transmit and receive circuits.

The Motherboard connects to the Control Panel board via connector PL5. In addition to serial data, this carries analogue signals from the panel Master Faders and Fade Duration controls and also power supplies. The serial output from IC28 pin 6 (Tx Data) is routed via buffer IC35/2 to terminal 3 of PL5, while data received from the Panel MPU appears on terminal 2 of the connector and is routed via buffer IC35/4 to pin 2 (Rx Data) of the ACIA.

5.6.1 Transmit/Receive Clock

The timing of the data transmitted and received via the serial link is determined by clock signals derived from a 4.9152MHz master oscillator. This is formed by crystal XL1, inverters IC13/2 and IC13/4, and their associated components. Its output (from IC13/4) is inverted and applied to divider IC12, the output of which (at 307.2kHz) provides the input to a second divider, IC9. The latter device produces outputs at 153.6kHz, 76.8kHz, 38.4kHz, 19.2kHz, 4.8kHz and 150Hz. The 76.8kHz signal is applied to the Tx Clk and Rx Clk inputs of IC28, while the 38.4kHz output is routed via buffer IC35/6 and PL5 terminal 1 to the Serial Communications Interface on the Control Panel Board. The ACIA and the Panel MPU respectively divide these clock signals by 16 and 8 to produce the correct clock rate for 4800 baud transmission.

5.7 ANALOGUE INTERFACE

The Analogue Interface consists of a Digital-to-Analogue converter (IC30), used to generate the multiplexed signal transmitted to the Multiplex Interface units, and an Analogue-to-Digital converter (IC26), which receives the multiplexed 'Manual Fader Wing' signal from the Multiplex Interface units and also the outputs from the four faders on the Control Panel board.

Two types of analogue output are possible: a two-wire system where the multiplexed analogue signal carries channel and frame sync pulses; and a four-wire system where the sync pulses are transmitted separately, on a balanced line. In the latter case, it is not possible to receive a multiplexed input from a manual fader wing.

5.7.1 Multiplexed Analogue Output

The multiplexed analogue output to the Multiplex Interface units is produced by D-A converter IC30, the output of which is fed via current-to-voltage converter IC51 and a unity-gain drive circuit consisting of Op-amp IC50 and transistors VT8 and VT9. The digital input to IC30 is provided by latch IC27, which is clocked by the pin 7 output of decoder IC31 each time the Motherboard MPU accesses address $8008. The inputs to the latch are data bus bits D0 - D7.

5.7.1.1 Reference Voltage

The reference voltage required by the D-A converter is derived from a 5.1V zener diode, D19, via inverting amplifier IC45/14. Resistors R58, R59 and R61 give a gain of slightly less than unity so that the output of IC45/14 is about -4.9V. This voltage is applied to the -Vref input of IC30 via RV2, which permits the adjustment of the full level analogue output.

5.7.1.2 Sync Pulses

Each time channel level data is loaded into IC27, the new channel is marked by an 8us Sync Pulse. Monostable IC46/5 is cleared on the front edge of the IC31 pin 7 output and then triggered on the back

edge, producing an 8us positive-going output. This pulse is routed via R66, R52 and VT7 to switch on transistor VT10, thus pulling the non-inverting input (pin 3) of IC50 down to -4.9V. At the end of the pulse VT10 switches off and the analogue channel level appears at the output. Diode D20 and resistor R90 ensure that VT10 switches off fully when the sync pulse is not present.

Following the last channel in each frame, a frame sync pulse is generated by the MPU on the CA2 line of PIA IC21. This pulse is slightly over 35us long and is applied to transistor VT6, the emitter of which is connected to the junction of R66 and R52. It thus controls VT7 and VT10 in a similar way to IC45/5, producing a -5V sync pulse on the analogue output. Following the frame sync pulse there is an interframe gap (analogue equals 0V) of at least 10us before the next frame begins. In practice this interframe gap will vary in length and it will rarely, if ever, be as short as 10us.

On systems using a four-wire analogue output link, terminal 4 of connector PL4 is connected to 0V and this pulls down the base of VT7, thus preventing the sync pulses appearing on the analogue output. The sync pulses are routed via line driver IC44/2 for use under these circumstances, appearing in complementary form on terminals 4 and 3 of connector PL3.

With the two-wire system in use, the output appearing on terminal 2 of connector PL3 takes the form shown in Fig. 5.7.1.1. The analogue channel level varies between +5V (full level) and 0V (zero), while the sync pulses are negative-going to -5V.

5.7.2 Analogue Input

The multiplexed analogue 'Manual Fader Wing' signal from the Multiplex Interface units is applied, via integrator R91-C2 and potential divider R65-R64, to amplifier IC45/1. The gain of this amplifier is adjustable by means of RV1 ('Man Full'). The output of IC45/1 is applied to an analogue data selector, IC52, the other inputs to which are the four fader outputs from the Control Panel board (see chapter 3); an additional analogue input (ANL IN),

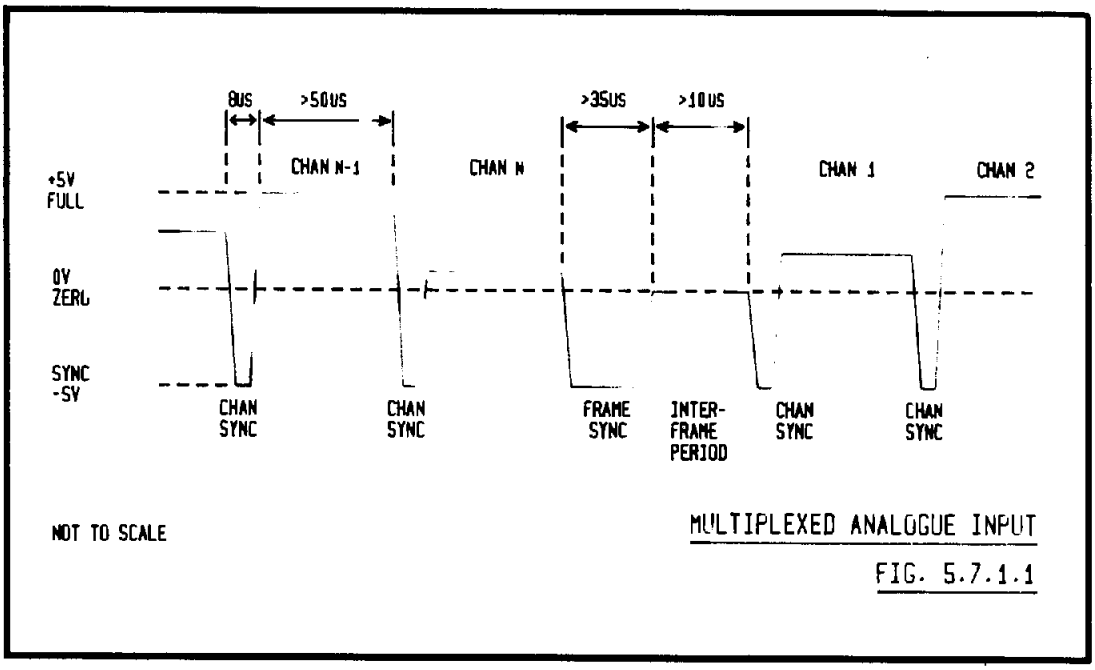


FIG. 5.7.1.1

provided for later expansion; ØV; and a D-A Test signal. The select inputs to IC52 are taken from lines PB5 - PB7 of PIA IC21 (see section 5.5).

IC52 is used in conjunction with capacitor C4Ø and buffer IC45/8 to form a sample-and-hold circuit which provides a stable input to A-D converter IC26. When a conversion is started, pin 14 (Busy) of IC26 is set low and, via buffer IC44/7, this inhibits IC52 so that the level of the selected input is stored on C4Ø. IC45/8 has a gain of slightly greater than unity and a small offset is applied via R6Ø to its inverting input to ensure that the faders are able to reach the full and zero settings.

The output of IC45/8 is applied to pins 3 and 4 of IC26. When the required analogue input has been selected, the conversion process is started by a low output from pin 6 of decoder IC31; this signal is produced when the MPU accesses address $8ØØA. 15us later the result of the conversion may be read via the same address, by means of data bus lines DØ - D7.

5.7.2.1 Fader Full Reference Voltage

The reference voltage supply to the control panel faders is taken from the junction of R58 and R59 (+4.9V - see section 5.7.1.1) via unity gain buffer IC45/7.

5.8 TAPE INTERFACE

The Tape Interface is provided by ACIA IC24 and its associated circuitry. The transmit clock applied to pin 4 of the ACIA is the 19.2kHz output from pin 5 of divider IC9 (see section 5.6.1); the ACIA divides this by 16 internally to give a data rate of 1200 baud. Data transmitted is converted into a CUTS format which uses two tones, 2400Hz to represent '1' and 1200Hz for '0'. At 1200 baud, each bit consists of two cycles at 2400Hz or one cycle at 1200Hz, depending on the bit state.

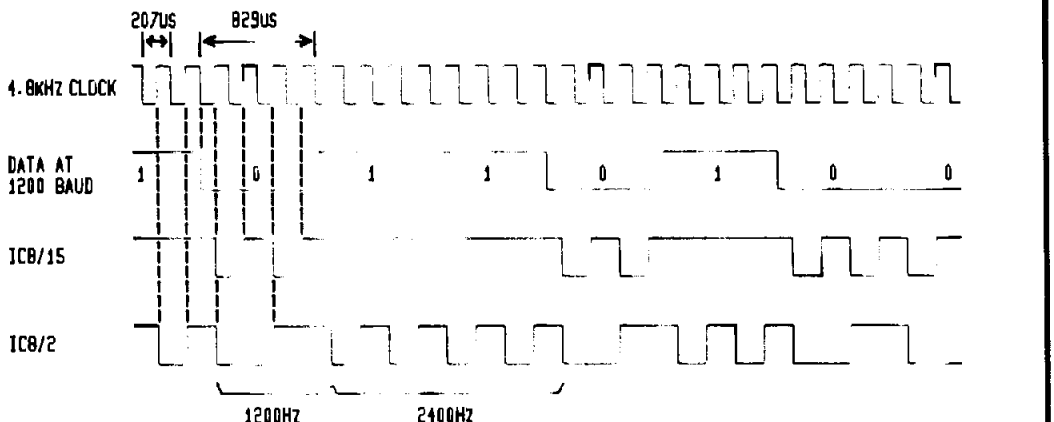
Because the tape speeds of low-cost cassette recorders are not, in general, very accurate, the receive clock must be derived from the incoming signal. This is achieved by means of an edge detector, and a phase-locked-loop operating in conjunction with a divider.

5.8.1 Transmitter Circuit

The Tx Data output of ACIA IC24 (at 1200 baud) is applied to the set input (pin 9) of J-K bistable IC8/15 and, via IC3/3 which acts as an inverter, to the J and K inputs of the same device. The output of IC8/15 is applied to the J and K inputs of a second bistable, IC8/2, and both bistables are clocked at 4.8kHz by the pin 2 output of divider IC9 (see section 5.6.1).

If the Tx Data signal is high (data = 1), pin 15 of IC8/15 is set high and IC8/2 therefore divides the clock frequency by 2, giving an output at 2400Hz. With Tx Data low (data = 0), IC8/15 is enabled and the two bistables then divide the clock by 4; the output is thus at 1200Hz. Typical waveforms are shown in Fig. 5.8.1.1.

The output from IC8/2 pin 2 is routed via a low-pass filter formed by R9, C6 and R5 and appears on terminal 1 of connector PL1.



TRANSMITTER WAVEFORMS

FIG. 5.8.1.1

5.8.2 Receiver Circuit

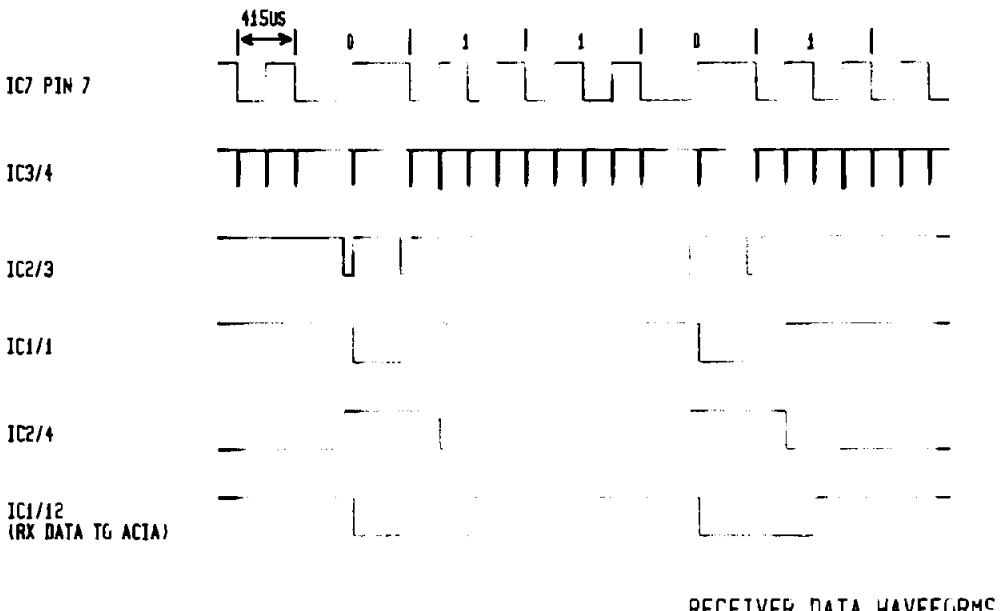
The incoming signal from the tape recorder appears on terminal 3 of connector PL1 and is applied to a filter formed by amplifier IC6, resistors R7 and R1Ø, and capacitors C9 and C1Ø. The filter removes mains hum and high frequency interference, and the gain of the amplifier is determined by R7 and R1Ø. The amplified and filtered signal is applied to comparator IC7 which acts as a Schmitt trigger, producing a rectangular waveform with the same form as that generated by the transmitter circuit.

The output of IC7 is applied to a circuit formed by IC3/1Ø, R6, C52 and IC3/4, which produces a short negative-going pulse for every edge, positive- or negative-going, of the input waveform. These pulses are inverted and applied to the reset input of counter IC5/14. The latter device is clocked by a 38.4kHz signal from pin 6 of divider IC9 (see section 5.6.1) and is inhibited by the output of IC2/3 when it reaches a count of 12.

If the incoming signal is at 2400Hz (data = 1), IC5/14 will be reset at a count of about 8 and pin 3 of IC2 will remain high. If,

however, the incoming signal is at 1200Hz (data = Ø), a count of 12 will be reached about three quarters of the way through each half-cycle and IC2/3 will produce a negative-going pulse.

The output of IC2/3 is applied to bistable IC1/1 which is clocked by the inverted output of IC3/4. The output of IC1/1 is therefore set low at the end of the first half-cycle of each data 'Ø' and will remain low until the end of the first half-cycle of the next data '1'. This signal is gated with the output of IC2/3 and applied to a second bistable, IC1/12, which extends this low signal by a further half-cycle (see Fig. 5.8.2.1) to ensure the correct timing of the data applied to ACIA IC24.

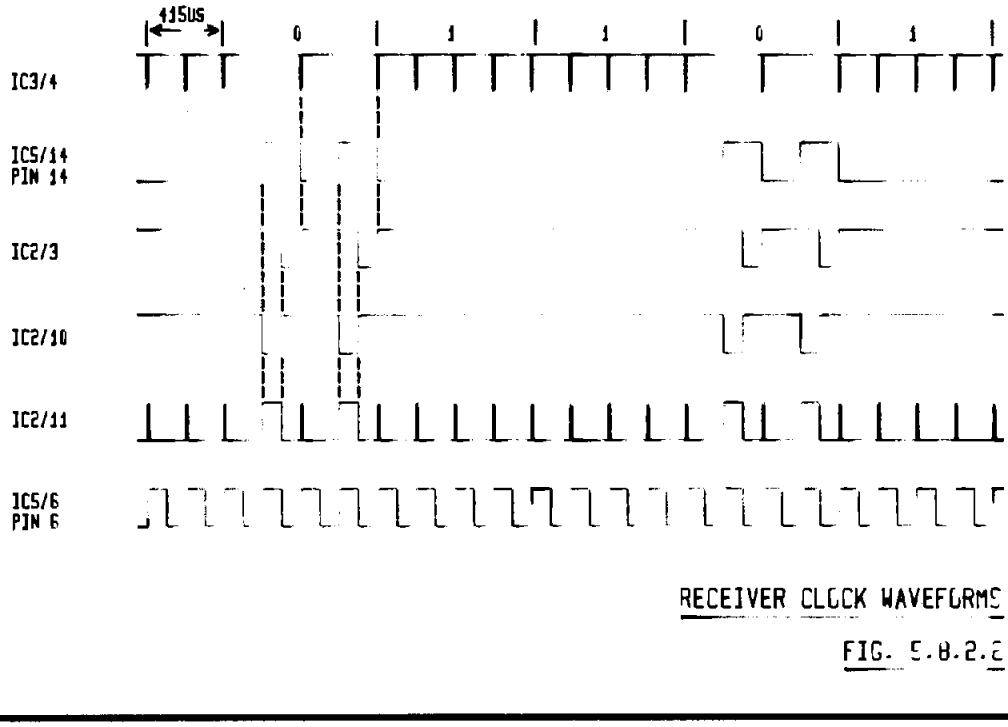


RECEIVER DATA WAVEFORMS

FIG. 5.8.2.1

Because the ACIA internally divides the Rx Clk signal by 16, a clock waveform at 16 times the data rate must be derived from the incoming signal. The output of IC2/3 is gated in IC2/1Ø with the signal from IC5/14 pin 14 and the resulting output is then gated (in IC2/11) with the negative-going pulses from IC3/4. This produces an

asymmetrical waveform, the positive-going edges of which appear at regular intervals, at a frequency corresponding to twice that which represents data '1' on the tape (i.e. about 4800Hz - see Fig. 5.8.2.2). This waveform is applied to one phase-comparator input of phase-locked-loop IC4.



RECEIVER CLOCK WAVEFORMS

FIG. 5.8.2.2

The other phase-comparator input is derived from the voltage controlled oscillator output (VCO - pin 4) of IC4, via divider IC5/6. The VCO output frequency will be constantly adjusted to keep the two input frequencies the same, but because of the divider this output frequency will be at about 76.4kHz. The required Rx Clk frequency (about 19.2kHz) is taken from pin 4 (Q1) of IC5/6.

5.8.3 Audio Test Circuit

If the CB2 line of PIA IC21 is set low, the output of bistable IC8/2 is connected to the tape input via transistor VT12. This permits the tape interface to be tested without the necessity of recording

and playing-back a test signal. Under these circumstances the gain of IC6 is determined by R28 and RlØ.

5.9 RESET CIRCUIT

The reset circuit is formed by transistors VTl - VT5, and their associated components. The circuit has two functions: firstly, to generate a reset pulse each time the equipment is switched on, thus ensuring that the MPU enters its start-up procedure correctly, and secondly, to inhibit processor operation if the voltages on the +5V and +15V rails vary by more than the allowed tolerance.

As the +5V rail becomes established at switch on, the voltage at the junction of C23, R37 and D17 will rise rapidly and VT5 will switch on; This pulls the Reset line low. When the rail reaches +3.6V, the voltage on the base of VT5 falls below Ø.7V, and this transistor switches off. The Reset line is then pulled high by a 1K resistor (RN2).

In normal operation, the emitter of transistor VTl is close to the +5V rail and the base of VT2 at about 1V; the latter transistor is therefore on and VT4 and VT3 off. If either rail starts to fall, the voltage on the base of VT2 will also fall until VT2 switches off; VT4 and VT3 will then switch on, pulling down the Reset line and inhibiting RAM write actions respectively. In addition, the MPU may be reset by means of a manual reset switch, SW3, which pulls down the base of VT2.

The Reset signal from VT4 is routed to the MPU (IC23) and the PIA (IC21) via the System Bus. This both ensures that devices on the daughter boards receive the Reset signal and allows the Motherboard MPU to be reset by a signal generated on a daughter board.

CHAPTER 6

POWER SUPPLY BOARD (Ref. 1830)

Drawing No. 6C26865

6.1 INTRODUCTION

The Ref. 1830 power supply board generates the three regulated supplies - +15V, +5V and -15V - required by the M24 Control Console. A similar board (Ref. 1863) is used in the M24Fx unit - see Drawing No. 6C28178.

The input to both types of board is a 17.5-0-17.5V a.c. supply produced by a transformer on the power supply assembly - see Drawing No. 7C26933 (M24) or 7C28189 (M24Fx). In each case, this input is rectified and smoothed, and applied to three regulator circuits, one for each output. Each regulator has its own rectifier and smoothing capacitor.

6.2 +15V AND -15V SUPPLIES

The +15V and -15V supplies are respectively produced by integrated circuit regulators REG1 and REG2. REG1 receives a rectified and smoothed input from D3, D4 and C8, while the input to REG2 is produced by D6, D7 and C7.

6.3 +5V SUPPLY

The +5V supply is produced by a switching regulator centred around integrated circuit REG3. This device contains a current-controlled oscillator; a temperature-compensated current-limiting circuit; a temperature-compensated voltage reference; and a high-gain differential comparator. These are used in conjunction with an external power transistor, VT1, and reservoir components TRX1 and C5. Regulation is achieved by means of negative feedback via potential divider R11/R4/R3, the output of which is compared with

the voltage reference (1.3V - pin 8) in order to control the output of the oscillator.

Current limiting is provided by means of parallel resistors R5-R1Ø. If, when VT1 is on, the voltage across these exceeds 33ØmV, the internal oscillator will shut down, switching VT1 off.

If, under fault conditions, the output voltage should rise above 5.6V, zener diode D5 will conduct. This has a crowbar effect and blows fuses FS1 and FS2.

IMPORTANT NOTE: All voltage measurements on the console must be made with reference to the ØV output of the Power Supply board; i.e. connector PL1 pins 4 and 5.

CHAPTER 7

VIDEO INTERFACE (Ref. 1834)

Drawing No. 6A26940

7.1 INTRODUCTION

The Video Interface board is an optional addition to the M24 Control Console and may be fitted in any one of the five 'daughter' board positions (SKT1 - SKT5) on the Motherboard. The board generates a video mimic-display signal which may drive a video monitor directly, or be converted into the form required by a monochrome television set by means of a UHF or VHF modulator attached to the associated connector panel.

The board carries a Cathode Ray Tube Controller (CRTC), 2Kbytes of Video RAM and a Character Generator.

7.1.1 Principle of Operation

The purpose of the Video Interface is to convert binary data supplied by the Motherboard MPU into a composite video and sync signal. This process is controlled by IC11, a CRT Controller device which generates line and frame sync pulses and Video RAM address signals. The latter control the storage of the display data by the MPU and its retrieval as each scan occurs. The display information (in ASCII code) is loaded into the Video RAM by means of a Multiplexed Direct Memory Access process (DMA) process.

The data retrieved from the RAM is applied to a character generator which produces a series of dot signals, line by line for each row of characters. These dot signals are combined with the Line and Frame sync pulses to produce the Composite Video signal.

7.1.2 Video Signal

The output of the board is a positive composite video signal with the following parameters:

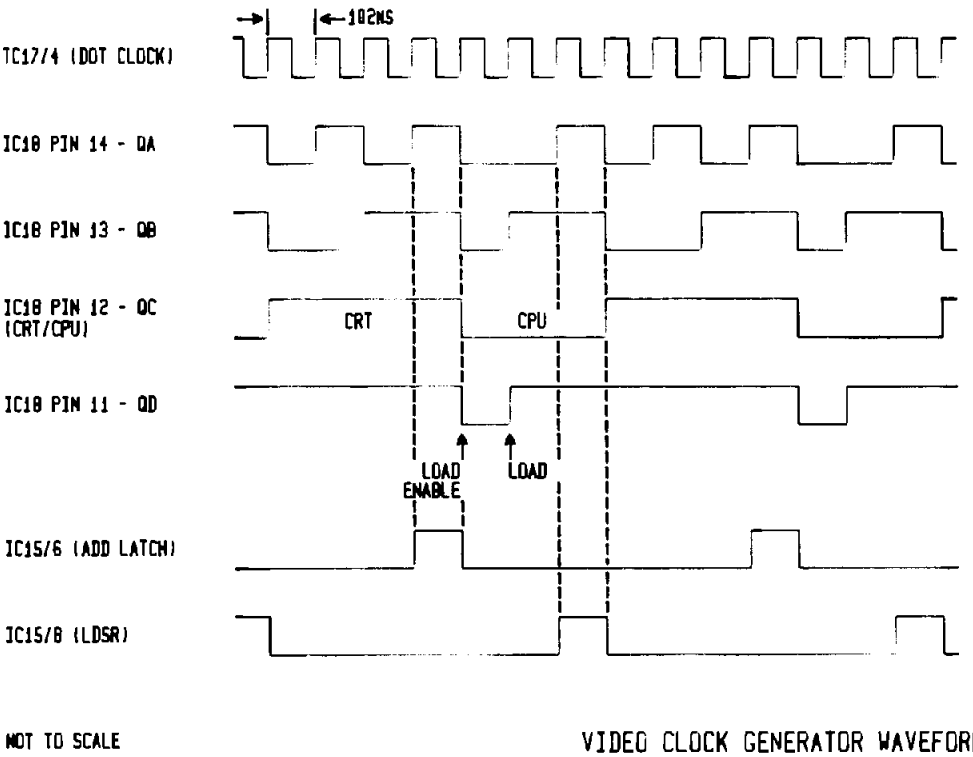
Impedance	:	75 ohms
Sync voltage	:	ØV
Black level	:	+Ø.3V
Dim White level	:	+Ø.7V
Peak White level	:	+1.ØV
No. of lines	:	312 at 5ØHz, non-interlaced
or	:	262 at 6ØHz, non-interlaced
Character Dot Rate	:	9.84375MHz
Characters/Line	:	64
Flyback blanking	:	17.7us
Character format	:	7 by 5 dot matrix
Lines/Character	:	9
Character lines	:	25

7.2 VIDEO INTERFACE ADDRESSES

Address lines A2 - A7 from the Motherboard MPU are applied to a wired-AND circuit formed by exclusive-OR gates IC6, IC5/3 and IC5/11. The circuit also receives 'E' (via IC4/3), VPA (via IC4/6) and R/W (via IC4/11). Links LK1 - LK6 permit any group of four addresses in the VPA area ($8ØØØ - $8ØFF) to be selected, those normally used being $8Ø18 - $8Ø1B (i.e. with LK1-3 and LK6 fitted and LK4 and LK5 not fitted). The output of the wired-AND circuit (CPREQ) selects the CRTC via timing circuitry which synchronises MPU write actions to the video system. The MPU may not read from the video system addresses.

7.3 VIDEO CLOCK GENERATOR

The clock pulses required by the Video system are generated by a 9.84375MHz oscillator formed by crystal XL1, inverters IC17/2 and IC17/4, and their associated components. The output of this oscillator is applied to counter IC18 and, as DOT CLK, to character generator IC13 (see section 7.4).



VIDEO CLOCK GENERATOR WAVEFORMS

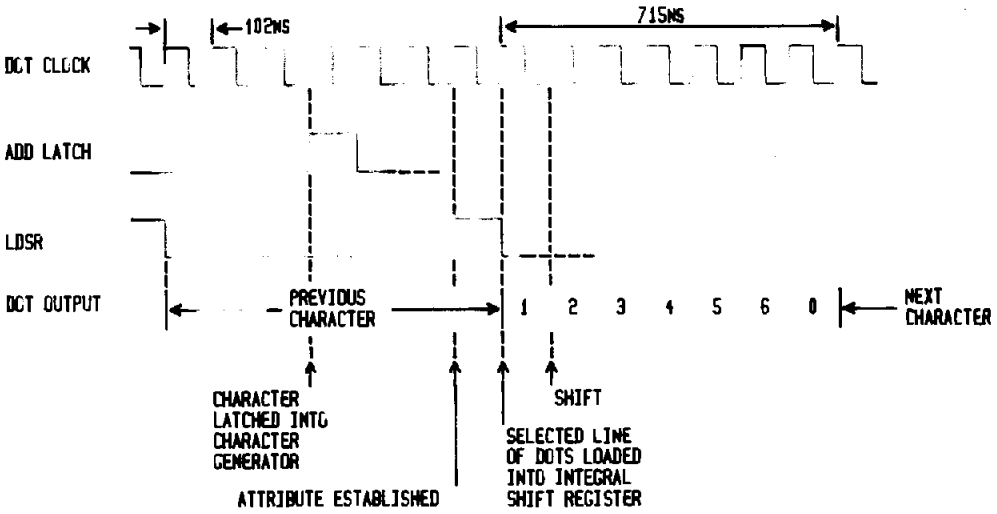
FIG. 7.3.1

IC18 divides the oscillator output by 7. Output D is applied to the Load Enable input (pin 9) so that, with D low the next clock edge will load the counter with 1010 ($A). It then counts up until D again goes low when the cycle repeats.

The C output of IC18 (CRT/CPU) is an asymmetrical waveform which is high for four DOT CLK pulses and low for three; it determines the CRTC scan rate and controls the relative timing of RAM read and write actions. The signal is also gated with the A and B outputs of IC18 to produce two further timing signals, ADD LATCH and LDSR (see Fig. 7.3.1).

7.4 VIDEO SCAN

The Cathode Ray Tube Controller (CRTC), IC11, generates Display Enable (DE), vertical and horizontal sync (VS and HS) and Video RAM address signals. The latter signals (MA0 - MA10) are used to scan



CHARACTER DOT TIMING

FIG. 7.4.1

the video RAM, IC12. Each RAM location consists of eight bits, six of which (DBØ - DB5) store the character to be displayed, while the remaining two (DB6 and DB7) determine the character 'attribute'.

As the RAM is scanned, bits DBØ - DB5 from each location in turn are applied to Character Generator IC13 and latched by the ADD LATCH pulse from IC15/6. The correct line of the character concerned is selected by a line counter and the dots forming this line are taken from an internal character ROM and loaded into a shift register on the LDSR pulse from IC15/8 (via inverter IC17/6); both the line counter and the shift register form part of the character generator. The dot output appears in serial form on pin 11 of IC13 and is routed via exclusive-OR gate IC5/8 to the video output circuit. The timing of these actions is shown in Fig. 7.4.1.

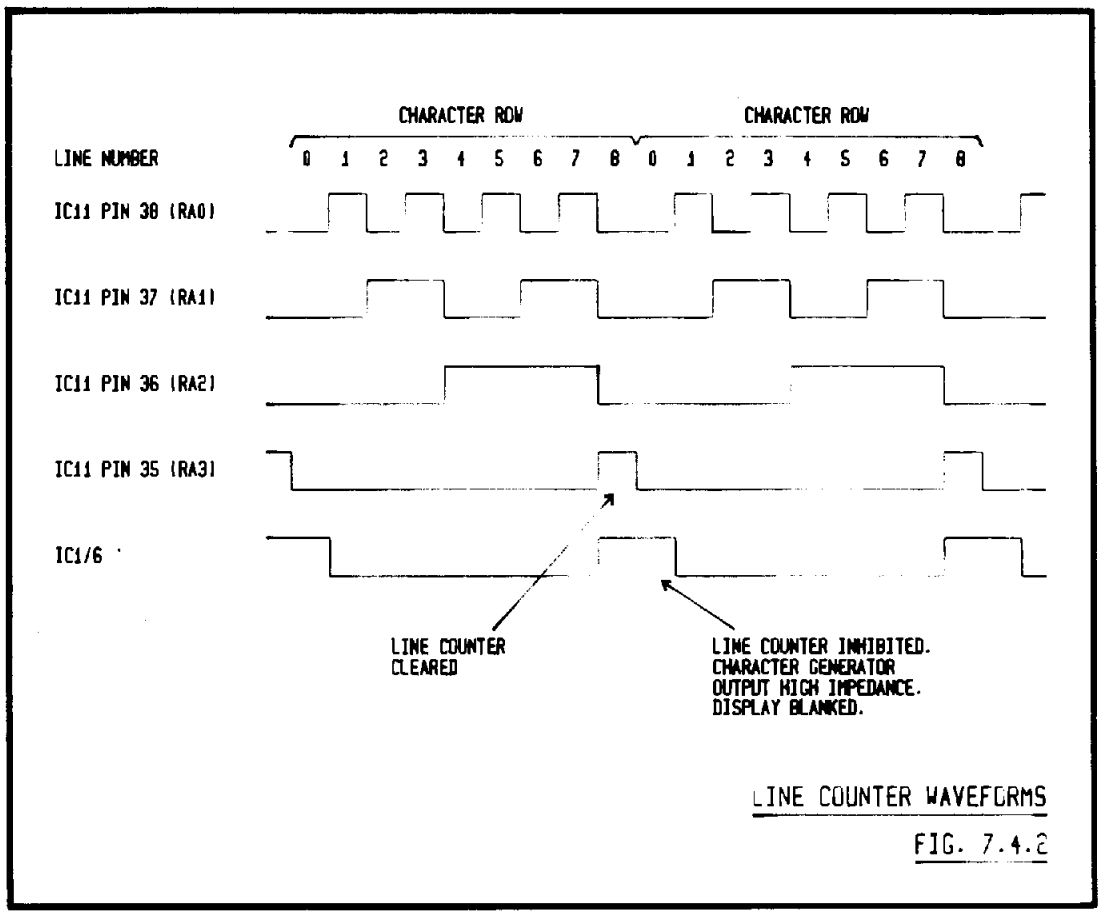
7.4.1 Character Line Synchronisation

Both the character generator and the CRTC contain line counters, that in the CRTC being used to synchronise the other to the display scan. Outputs RAØ, RA1 and RA2 from IC11 are gated together in NOR gate IC1/6 and the output of this is applied to transistor VT2 and

to the Output Enable and, via inverter IC7/1Ø, Clock Control inputs of IC13. As a result, whenever RAØ-2 are all low (i.e. during the first and last lines of each row of characters - see Fig. 7.4.2) the line counter in IC13 is inhibited and the character generator is high impedance. At the same time, VT2 is conducting, pulling the output down to ØV.

During the last line of each character row (line 8), RA3 from IC11 will be high (see Fig. 7.4.2) and, via IC17/12, this clears the character generator line counter in preparation for the next row.

The IC13 line counter is clocked by the pin 1 output of latch IC14/16. The latter receives the DE (Display Enable) signal from the CRTC and is clocked by ADD LATCH (see Fig. 7.5.1).



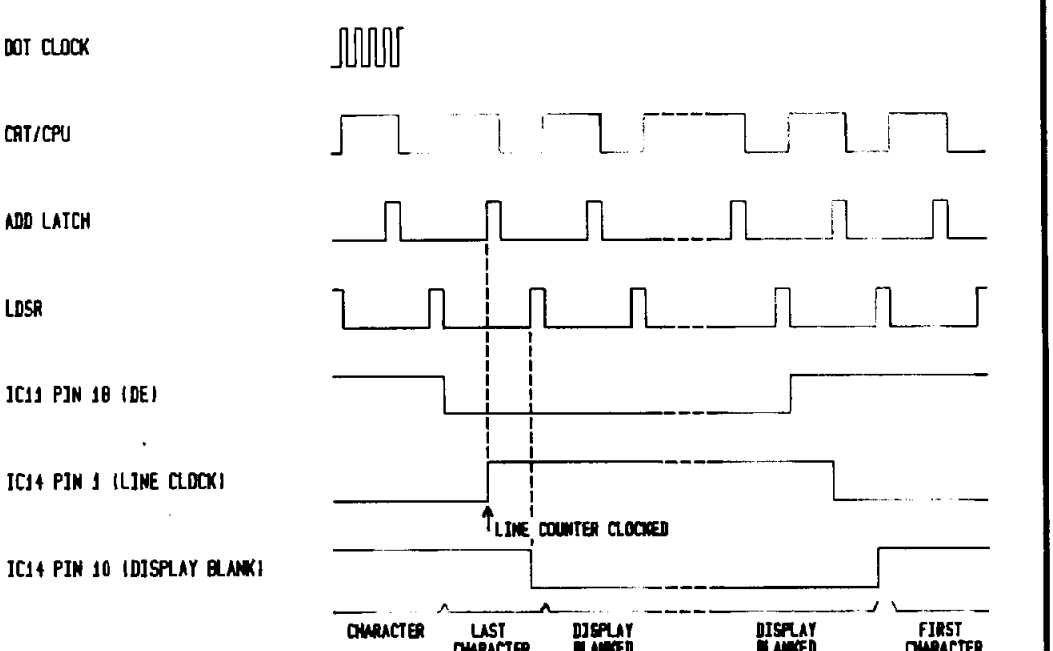
LINE COUNTER WAVEFORMS

FIG. 7.4.2

7.5 VIDEO OUTPUT

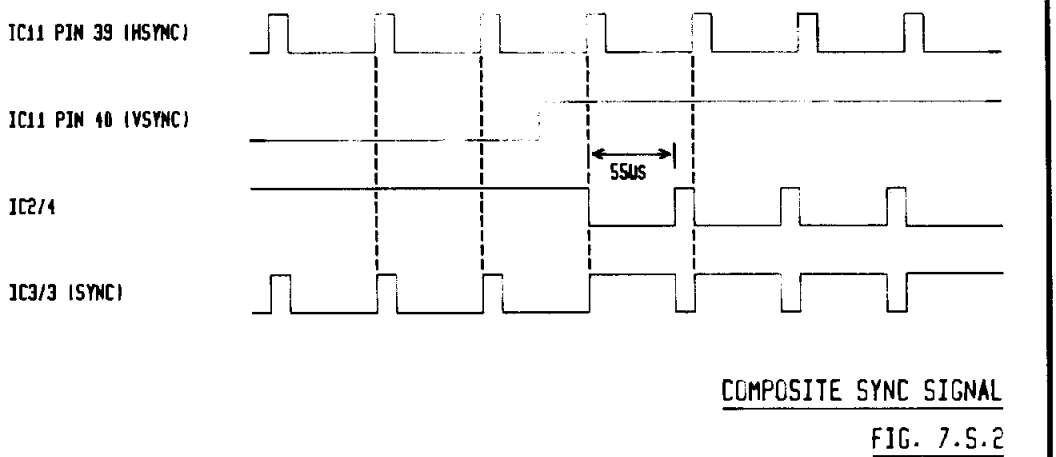
The output from IC5/8 is applied, via diode D1, to emitter follower VT1, which produces the video signal. When the Character Generator output is at 0V, or the output is blanked (either by VT2 or by a low output from IC14/10, via diode D4), D1 is back biased. The base of VT1 is then held at about 1V by R6 and R4, thus establishing a black level of about 0.3V on the output. Note that the +5V supply to the video output circuit is derived from the +15V rail by R7 and D2.

Note: The Blanking signal is derived from the DE output of the CRTC via cascaded latches IC14/16 and IC14/10. These are clocked by ADD LATCH and LDSR respectively and ensure that the Blanking signal does not appear until the last character has been output to the screen (see Fig. 7.5.1).



DISPLAY BLANK WAVEFORMS

FIG. 7.5.1



COMPOSITE SYNC SIGNAL

FIG. 7.5.2

The video line and frame sync pulses are produced by -NOR gate IC3/3, the output of which controls an exclusive-OR gate (IC5/6) in the video output circuit. The latter gate clamps the base of VT1, thus reducing the video output to ØV.

While the VSYNC output (pin 4Ø) of IC11 is low, monostable IC2/4 is cleared and its pin 4 output is high. Under these circumstances, line sync pulses are produced by routing HSYNC from pin 39 of IC11 via inverter IC7/6 to -NOR gate IC3/3. When VSYNC goes high at the end of each frame, IC2/4 is no longer cleared and is triggered on the leading edge of HSYNC, producing a 55us negative-going output. This is applied to IC3/3 to produce the frame sync signal. When IC2/4 times-out, the output of IC3/3 goes low for a short period before the next HSYNC edge (see Fig. 7.5.2).

7.5.1 Character Attributes

Bits DB6 and DB7 from the Video RAM are applied to latches IC16/16 and IC16/15 respectively, both of which are clocked by ADD LATCH. The resulting outputs are applied to a second pair of latches, IC16/1Ø and IC16/9, which are clocked by LDSR. This arrangement ensures that the attribute is established on the video output at the correct time, relative to the character dot output (see Fig. 7.4.1).

When a dim character is to be output, DB6 and DB7 are both high and NAND gate IC3/8 is fully enabled by the outputs of latches IC16/10 and IC16/9. IC3/8 therefore produces a low output which is connected, via diode D5 and resistor R8 to the output of IC5/8. The result is similar to that produced by the Display Blank signal, but because of D5 and R8 the output is not reduced as far as black level.

Inverse characters are produced if DB6 is low and DB7 high. The outputs from pin 10 of IC16/10 and pin 8 of IC16/9 enable -NAND gate IC1/12 and the output of the latter is applied to exclusive OR gate IC5/8. The character generator output is then fed to transistor VT1 in inverted form.

Characters may be made to flash on and off by setting DB6 high and DB7 low. The outputs from pin 11 of IC16/10 and pin 9 of IC16/9 enable -NAND gate IC1/8 and this, in turn, partially enables IC3/6. The second input to the latter gate is the BLINK CLK signal, derived from VSYNC by counter IC10. Whenever IC3/6 is fully enabled, its low output pulls down the output of IC5/8 via diode D3.

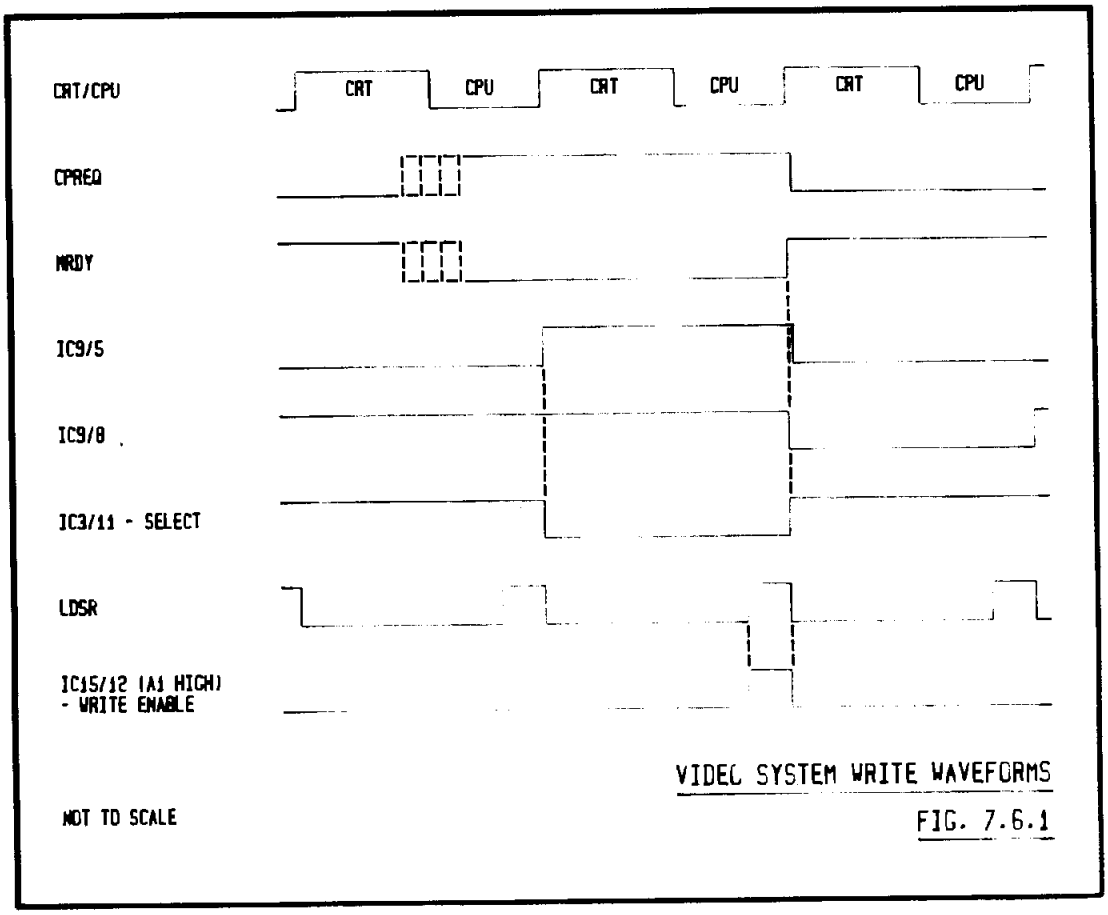
7.6 MPU ACCESS TO THE VIDEO SYSTEM

Because the Video scan must be continuous, the Motherboard MPU may only write to the video interface in the unused time between CRTC read actions; the process is controlled by the CRT/CPU waveform from counter IC18. When this signal is high, display address signals from the CRTC are applied to the RAM and the appropriate character is read for display (inverted CRT/CPU is applied to pin 20 of IC12 to control the RAM outputs). When CRT/CPU is low an 'update address', taken from two registers within the CRTC, appears on MA0-MA10 and the RAM outputs are disabled; at the same time, Bus buffers IC8 are enabled by CRT/CPU, giving the MPU access to both the CRTC and the Video RAM.

The operation of the Motherboard Processor and the Video Interface are not synchronised and the MPU must therefore wait until the correct time in the CRTC cycle before performing a write action. When the MPU writes to any of the four Video address locations

($8018 - $801B), the combined output of the wired-AND circuit described in section 7.2 becomes high (CPREQ). This signal partially enables NAND gate IC4/8 and triggers monostable IC2/5 (4.5us); the positive-going output produced by the latter fully enables IC4/8. The output of the gate drives the Bus MRDY line and this causes the processor cycle to be stretched until the write action is complete.

The output from the wired-AND circuit is also applied to the D and Clear inputs of bistable IC9/5. The latter is clocked by CRT/CPU and on the next positive-going edge of this waveform it produces a high output on pin 5, thus enabling NAND gate IC3/11 (see Fig. 7.6.1). IC3/11 is already partially enabled by a high output from IC9/8 and its output therefore goes low. This signal (Select) is applied to the Chip Select input (CS - pin 25) of the CRTC and, inverted by IC7/8, to AND gate IC15/12 which generates the RAM Write Enable pulse.



VIDEC SYSTEM WRITE WAVEFORMS

FIG. 7.6.1

Bistable IC9/8 is also clocked by CRT/CPU and on the next clock edge its pin 8 output will be set low, terminating the Select signal by inhibiting IC3/11 and clearing monostable IC2/5. The latter device inhibits IC4/8, thus terminating the MRDY signal and allowing the processor cycle to complete. When this takes place the Bus 'E' signal will go high, setting CPREQ low and clearing IC9/5. On the next positive-going edge of CRT/CPU, pin 8 of IC9/8 will be set high, returning the system to its quiescent state.

7.6.1 Loading Display Characters into the RAM

As described in the previous section, an 'update address' appears on the MA0-MA10 lines of the CRTC during the low, CPU portion of the CRT/CPU waveform. This address is taken from two registers (R18 and R19) within the CRTC and these may be loaded by the MPU with the address of any location in the Video RAM. The selected display location may then be accessed by writing to Motherboard address $8019.

When the Motherboard MPU writes to this address, the Select signal is generated and the processor cycle stretched as described in the previous section. In addition, Bus A1 is high (A1=0) and this and Select partially enable AND gate IC15/12. When LDSR from IC15/8 goes high (see Fig. 7.6.1), IC15/12 will become fully enabled and the resulting output, inverted by IC17/10 and applied to pin 21 (WE - Write Enable) of IC12, causes the information on the Data Bus to be written into the selected RAM location.

In order to avoid the necessity of reloading the update address registers each time a different Video RAM location is to be accessed, the CRTC includes a facility which allows the update address to be incremented automatically each time a RAM write action takes place. Register R31 in the CRTC is a 'dummy' register which, if accessed at the same time as the RAM, will cause this increment action to occur. In order to use this facility, the MPU loads the update registers and then sets the register pointer (address $801A) to 31, before starting to write to the RAM. The Select signal, applied to pin 25 of IC11, ensures that the CRTC is accessed at the same time as the Video RAM.

7.6.2 CRTC Initialisation

Addresses $801A and $801B in the Motherboard address map are assigned to the CRTC's internal registers. These are set-up during system initialisation to produce the required screen format (see section 2.2.5). The data stored in the registers is as follows:

Register	0 = $5A	
	1 = $40	
	2 = $47	
	3 = $87	
	4 = $21	($50Hz) or $1B ($60Hz)
	5 = $06	($50Hz) or $04 ($50Hz)
	6 = $19	
	7 = $1C	($50Hz) or $1A ($60Hz)
	8 = $88	
	9 = $08	
	10 = $20	turn Cursor control OFF
	11 = $00	
	12 = $00	
	13 = $01	
	14 = $00	
	15 = $00	
	16 = Not used	
	17 = Not used	
	18 =	
	19 =	Update Address Register
	31 =	Address update dummy register

Note: The required timing is selected by the System Configuration Switches on the Motherboard.

7.7 VIDEO MODULATOR BOARD

Drawing No. 6C28009

The video modulator is mounted on a small printed circuit board attached to the Video Connector Panel. The video input is routed to the modulator via emitter follower VT1. Note that the +5V supply is taken from the video output circuit on the Video Interface board (see section 7.5).

CHAPTER 8

MULTIPLEX/DEMULTIPLEX BOARD (Ref. 1828)

Drawing No. 6A26850

8.1 INTRODUCTION

Each Multiplex Interface unit contains a single Multiplex/Demultiplex Board which generates the dimmer drive outputs for 24 channels and receives control inputs from the corresponding channels on the Manual Fader Wing. The control inputs are multiplexed and transmitted to the Control Console, while the multiplexed analogue signal from the Console is sampled to extract the levels for the channels controlled by the board; these levels are stored on capacitors. The levels are refreshed or updated approximately every 50ms.

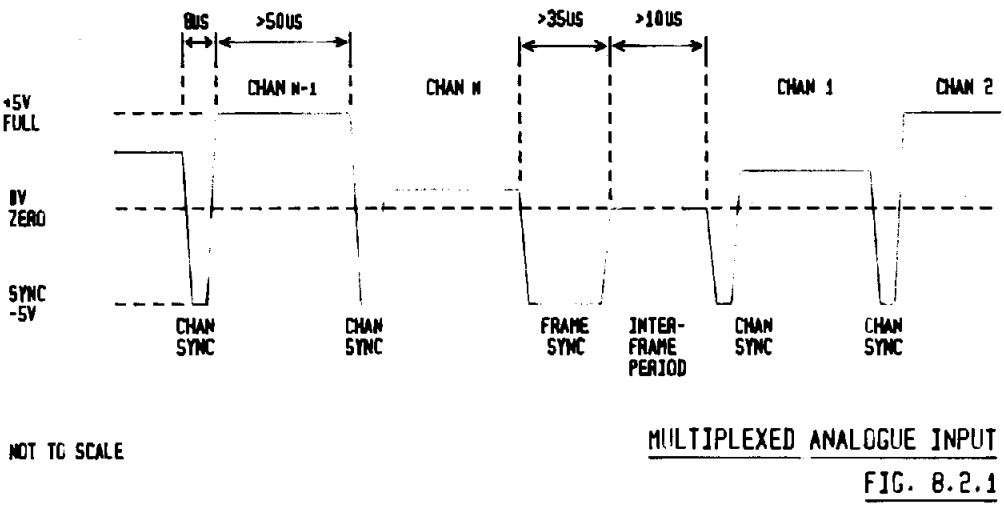
8.2 MULTIPLEXED ANALOGUE INPUT

The incoming multiplexed analogue signal appears on terminal 4 of connector PL1 and, terminated by capacitor C2 and resistors R50 and R51, is applied to unity-gain buffer IC3/7. The signal takes the form shown in Fig. 8.2.1. The analogue channel level varies between +5V (full level) and 0V (zero), while the sync pulses are negative-going to -5V.

Some equipment may use an alternative, four-wire system which has separate analogue and sync signals. In the latter case, the sync signals appear on terminals 5 and 6 of PL1 and are applied to Op-amp IC3/8 which acts as a differential line receiver.

8.2.1 Channel Sync Pulses

The output of IC3/7 is applied, via diode D21, to IC3/8 which, in the case of the two-wire system, acts as a simple inverting amplifier with a gain of 2. The diode provides isolation from the analogue signals when using the four wire system.



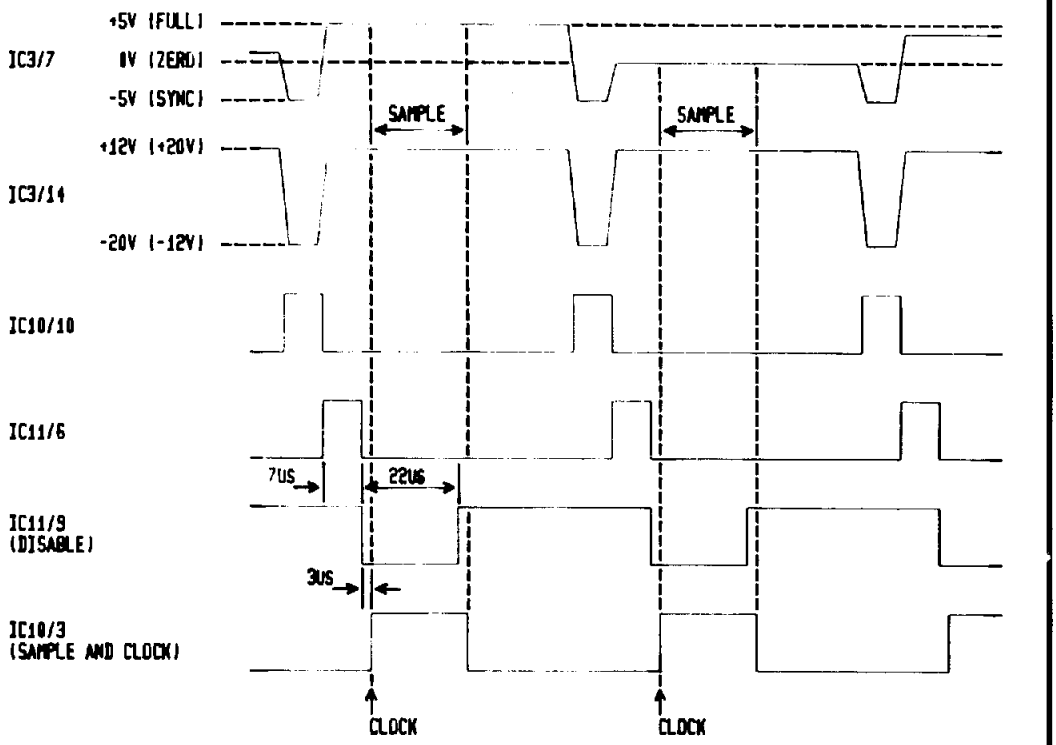
MULTIPLEXED ANALOGUE INPUT
FIG. 8.2.1

The output of IC3/8 is routed via a third Op-amp, IC3/14, which has positive feedback via R28, giving a Schmitt trigger action. The output of the latter is applied, via C74, to -NOR gate IC10/10. The capacitor provides a.c. coupling, thus allowing the signal to be converted to the CMOS voltage levels required by the gate. Diodes D10 and D11 ensure that the permissible input levels are not exceeded.

The negative-going edges of the output from IC10/10 (i.e. the trailing edges of the sync pulses) trigger monostable IC11/6, which produces a 7us positive-going pulse on pin 6 (see Fig. 8.2.2). On the trailing edge of the latter signal, IC11/9 is triggered and the negative-going output (pin 9) of this monostable, routed via delay circuit R44/C15 (3us) and Schmitt trigger IC10/3, enables analogue switch IC4/2.

8.2.2 Analogue Sampling

IC3/7 also feeds Op-amp IC3/1 which, depending on whether the dimmer drive outputs are to be positive- or negative-going, may be configured as either inverting or non-inverting by means of link LK2. In either case the gain of the device depends on the required control voltage range and is set by resistors R48 and R34. The



ANALOGUE SAMPLING WAVEFORMS

FIG.8.2.2

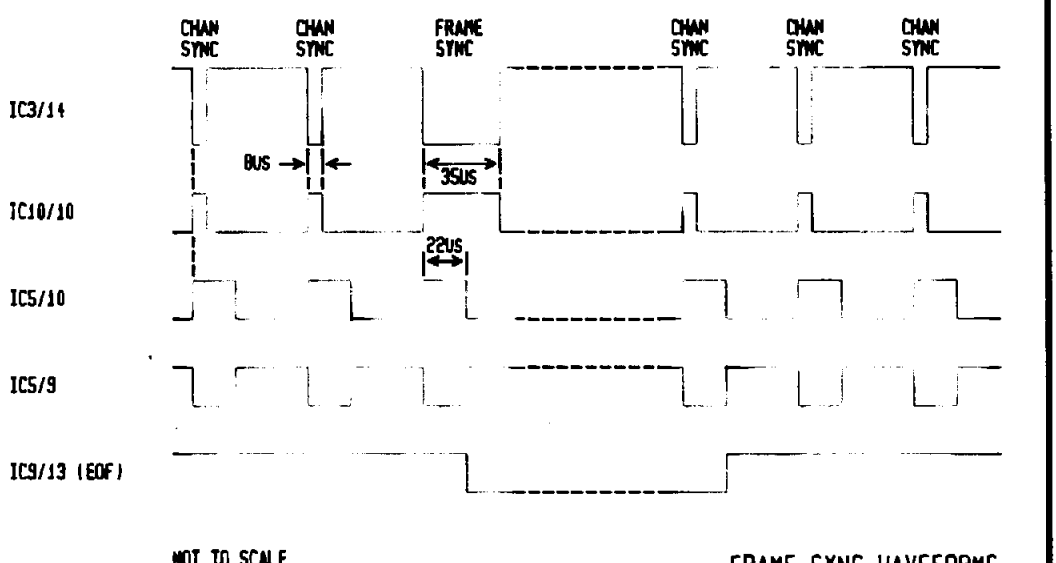
output of IC3/1 is routed via analogue switch IC4/4 (which is enabled if a multiplexed analogue signal is being received) and buffer IC2/8 to the analogue input of IC4/2. When the latter device is enabled, the output of IC2/8 is applied to capacitor C1, which therefore charges to the analogue level of the channel currently being sampled (see Fig 8.2.2).

8.2.3 Output Enable

The output of Schmitt trigger IC10/3 is also applied to the clock input of a counter formed by IC7, IC8/10, IC8/11, IC9/1, IC15 and IC16 (see section 8.4). This counter produces outputs which are used to route the sampled analogue signal to the appropriate dimmer drive circuit. The counter outputs change on the front edge of the clock pulse.

One of the outputs produced by the counter is a Card Enable signal which is high for the transmission period of the 24 channels served by the board. This is gated with the output of IC11/9 (Disable) in NAND gate IC8/3 and the output of the latter enables one half of decoder IC6 (on pin 1). IC6 receives select inputs (C3 and C4) from the counter and produces a low output on one of pins 4, 5, or 6. These are each connected to the enable input of one of three 8-channel analogue demultiplexers which receive select signals CØ - C2 from the counter. The analogue input to the demultiplexers is from Op-amp IC2/4, the input to which is the analogue voltage stored on C1.

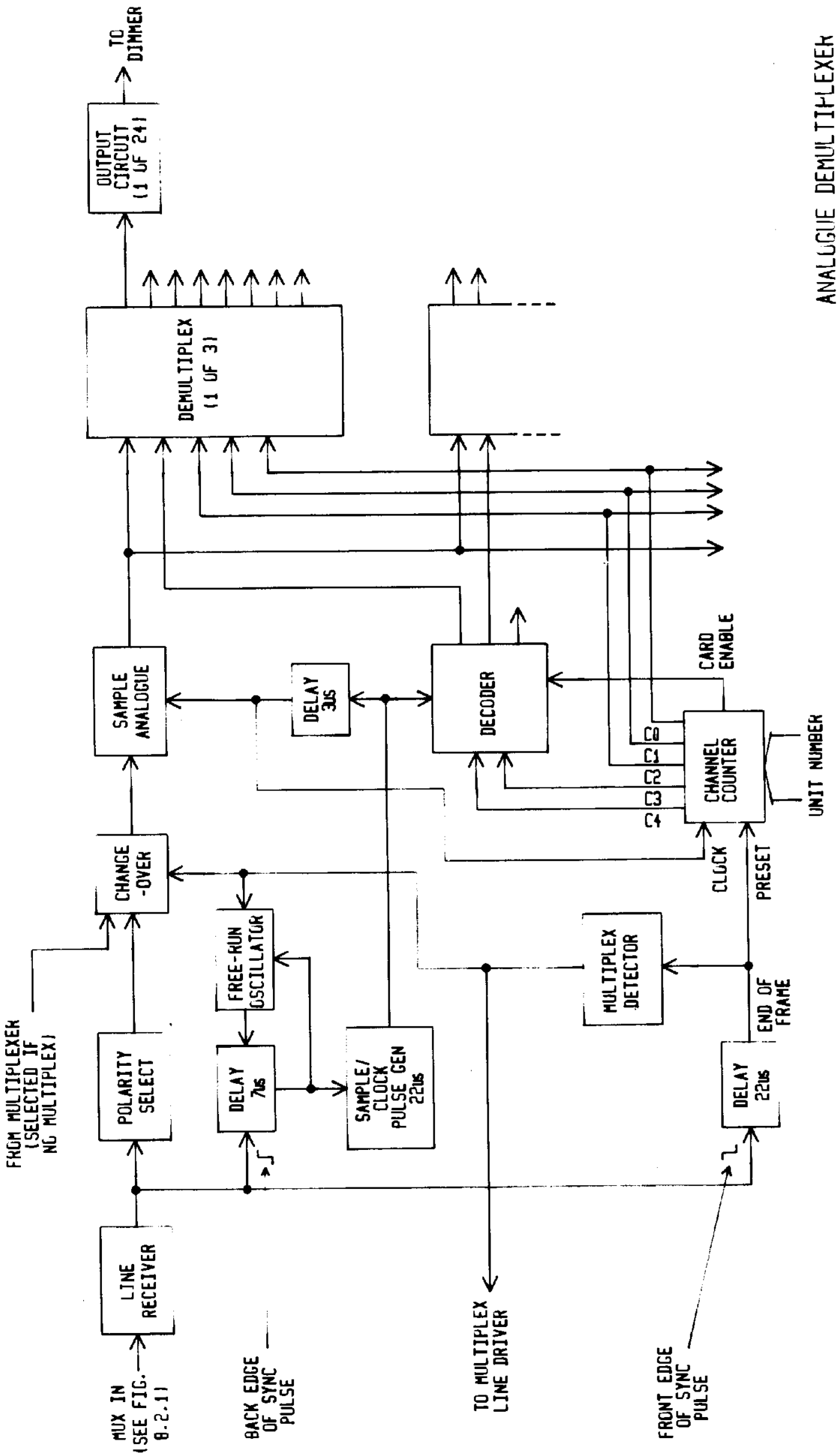
The Disable signal from IC11/9 inhibits NAND gate IC8/3 during the sample period for each channel (see Fig. 8.2.2) and thus, via decoder IC6, disables the selected demultiplexer. This ensures that the voltage on C1 is not connected to the selected output until it has attained a stable state.



NOT TO SCALE

FRAME SYNC WAVEFORMS

FIG. 8.2.3



ANALOGUE DEMULTIPLEXER

FIG. 8.2.4

8.2.4 Dimmer Drive Outputs

During the Output Enable period (i.e. while IC8 pin 3 is low) the output of IC2/14 is applied, via the selected analogue demultiplexer, to one of twenty four capacitors (C17 - C4Ø). These each provide the input to a unity gain Op-amp which, via a resistor and a diode, feeds the dimmer drive line for the corresponding channel. The diodes allow the outputs of Tempus M24 to combine on a Highest-takes-precedence basis with those of other control systems, while the resistor provides current limiting and high-voltage protection in the event of a fault.

When IC8 pin 3 goes high, the analogue demultiplexer channel is disabled and presents a high impedance to the capacitor. As the input to the Op-amp is also high impedance, the capacitor retains its charge until refreshed on the next frame of the multiplexed analogue signal.

8.2.5 Frame Sync

At the end of each frame of channel level data, a Frame Sync pulse with a duration of at least 35us appears on the multiplexed analogue input. This is detected by means of monostable IC5/1Ø (22us), which is triggered on the leading edge of every sync pulse by the output of IC1Ø/1Ø. The output from pin 9 of IC5/1Ø is applied to the clock input of bistable IC9/13, the D input to which (pin 9) is the sync signal from IC3/14 - via C74. On the trailing edge of the 22us pulse from IC5/1Ø, IC9/13 is clocked and its pin 13 output is set low or high, depending on the state of its D input. In the case of the Channel Sync pulses, IC3 pin 14 returns high after 8us and IC9 pin 13 is set high. When the longer Frame Sync pulse appears, however, IC3 pin 14 is still low after 22us and pin 13 of IC9 is set low.

The end of Frame (EOF) signal thus produced is used to reset the channel counter as described in section 8.4, and to trigger multiplex detector IC5/6 (see section 8.5).

8.3 MULTIPLEXED ANALOGUE OUTPUT

8.3.1 Analogue Inputs

The control signals from the Manual Fader Wing are applied, via potential dividers, to the inputs of three analogue multiplexer devices: IC17, IC18 and IC19. These receive select signals C0-C2 from the counter (see section 8.4) and are each enabled by one output from the second half of decoder IC6 (i.e. IC6 pins 12, 11 and 10). The latter device is enabled by NAND gate IC8/4, which is in turn enabled by the Card Enable signal from the counter and a Power OK signal from IC10/11 (see section 8.7).

The selected control signal provides the input to Op-amp IC2/1, which has a gain of 11 to restore the signal to its original level. The feedback path also includes two diodes, D2 and D3, which compensate for the diodes in the outputs of the Manual Fader Wing. Which diode performs this function depends on the polarity of the control inputs, D3 being used in the case of negative-going signals and D2 for positive-going. An offset applied via resistor R121 (negative) or R120 (positive) ensures that the appropriate diode remains in forward conduction at all times.

During the period when the input selection is changing, the pin 3 input of IC2/1 is connected to 0V, via analogue switch IC4/11, to prevent spurious signals on the output. IC4/11 is controlled by the pin 10 output of monostable IC5/10 (22us), which is triggered on the front edge of each sync pulse by the output of IC10/10 (see section 8.2.5 - Frame Sync).

8.3.2 Multiplexed Output

The output of IC2/1 feeds Op-amp IC1/6 which, depending on whether the inputs from the Manual Fader Wing are positive- or negative-going, may be configured as either inverting or non-inverting by means of link LK1. IC1/6 controls FETs VT4 and, via transistor VT3, VT5, and these drive the Multiplex Output line; the latter output is fed back via R24 to the inverting input of the Op-amp.

8.3 MULTIPLEXED ANALOGUE OUTPUT

8.3.1 Analogue Inputs

The control signals from the Manual Fader Wing are applied, via potential dividers, to the inputs of three analogue multiplexer devices: IC17, IC18 and IC19. These receive select signals CØ-C2 from the counter (see section 8.4) and are each enabled by one output from the second half of decoder IC6 (i.e. IC6 pins 12, 11 and 1Ø). The latter device is enabled by NAND gate IC8/4, which is in turn enabled by the Card Enable signal from the counter and a Power OK signal from IC1Ø/11 (see section 8.7).

The selected control signal provides the input to Op-amp IC2/1, which has a gain of 11 to restore the signal to its original level. The feedback path also includes two diodes, D2 and D3, which compensate for the diodes in the outputs of the Manual Fader Wing. Which diode performs this function depends on the polarity of the control inputs, D3 being used in the case of negative-going signals and D2 for positive-going. An offset applied via resistor R121 (negative) or R12Ø (positive) ensures that the appropriate diode remains in forward conduction at all times.

During the period when the input selection is changing, the pin 3 input of IC2/1 is connected to ØV, via analogue switch IC4/11, to prevent spurious signals on the output. IC4/11 is controlled by the pin 1Ø output of monostable IC5/1Ø (22us), which is triggered on the front edge of each sync pulse by the output of IC1Ø/1Ø (see section 8.2.5 - Frame Sync).

8.3.2 Multiplexed Output

The output of IC2/1 feeds Op-amp IC1/6 which, depending on whether the inputs from the Manual Fader Wing are positive- or negative-going, may be configured as either inverting or non-inverting by means of link LK1. IC1/6 controls FETs VT4 and, via transistor VT3, VT5, and these drive the Multiplex Output line; the latter output is fed back via R24 to the inverting input of the Op-amp.

In the inverting mode, the gain of IC1/6 is determined by resistors R23 and R24, while in the non-inverting mode the Op-amp has unity gain and R23 and R2 form a potential divider in its input. In either case, R23 is chosen to give an output range of ØV to +5V on the source of VT4.

8.3.3 Output Disable

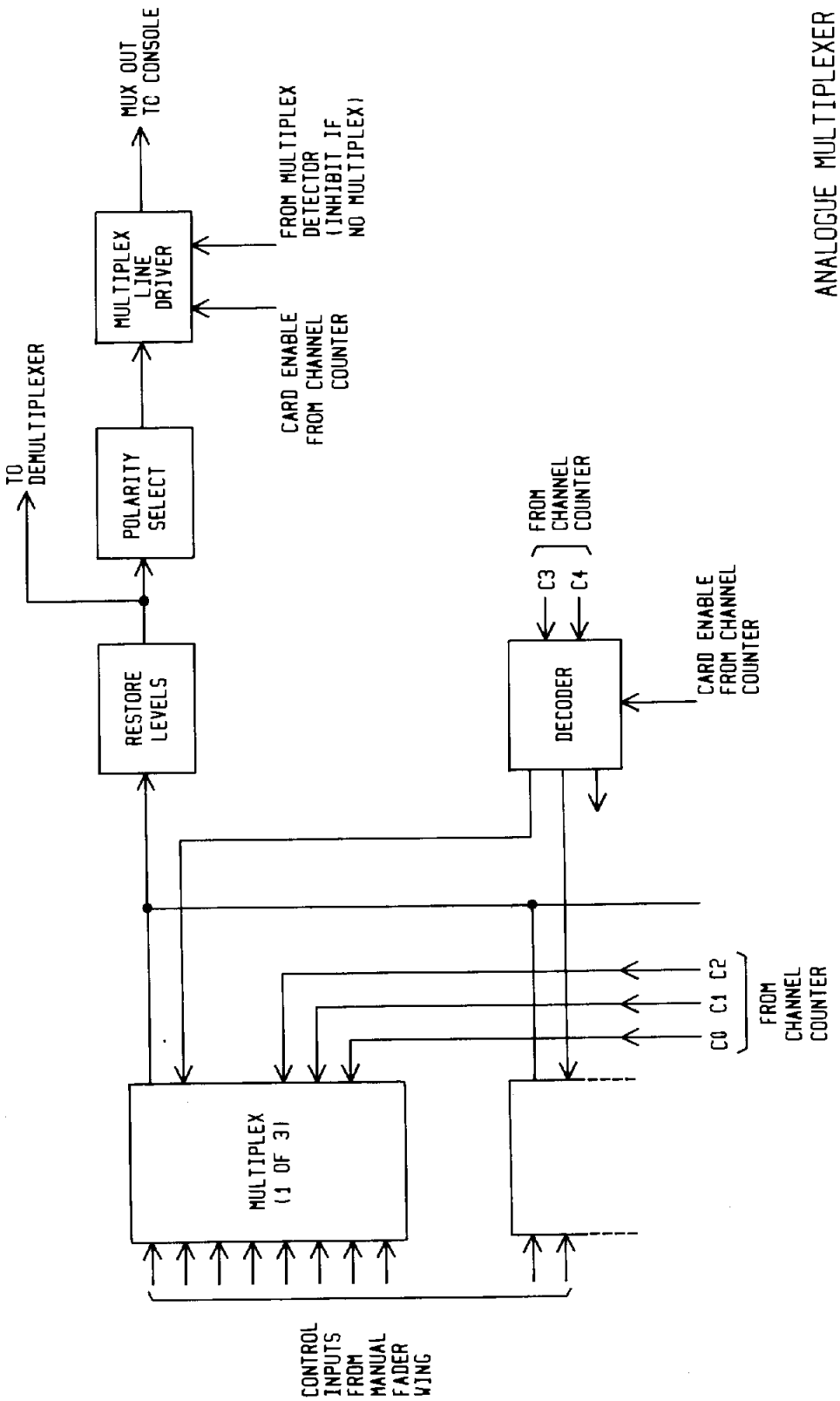
The above describes the operation of the multiplexer during the period when the board is enabled, i.e. while the levels of the channels served by the board are being transmitted. During the remainder of the frame, however, other boards may be transmitting channel levels and both VT4 and VT5 must be switched off to permit the other boards to use the common multiplex output line.

The Card Enable signal from the counter is connected via diode D5Ø and transistor VT6 to the bases of two transistors, VT1 and VT2. While the channels served by the board are being scanned, Card Enable is high, D5Ø is back-biased and both VT1 and VT2 are off. When Card Enable goes low, however, the bases of VT1 and VT2 are pulled down via D5Ø and VT6, and the transistors switch on. VT2 pulls up the base of VT3, thus switching off VT5, and VT1 pulls up the inverting input of IC1/6, which thus produces a low output, switching off VT4. VT6 ensures the correct operation of the circuit on both positive and negative versions of the board, its working point being set by resistors R11 and R12.

Note: A second diode, D49, connected to the junction of D5Ø and VT6 is used to disable the output when no multiplexed input is being received. See section 8.5.

8.3.4 MUX OK Indicator

The signal on the collector of VT1 is also applied to a circuit which controls the MUX OK indicator, LED2. This circuit is formed by Op-amp IC2/7, zener diode D55, transistor VT13 and their associated components.



ANALOGUE MULTIPLEXER

FIG. 8.3.1

With VT1 off (card enabled), the non-inverting input of IC2/7 is pulled down via R118 and the 0V output of the Op-amp rapidly discharges C73 via D54. Under these circumstances VT13 remains off and the LED is illuminated as a result of current flowing via R116. If the card is not enabled, the input to IC2/7 is pulled high by VT1; D54 is then back-biased and C73 begins to charge via R117.

In order to turn on VT13, and thus by-pass LED2 switching it off, the voltage on C73 must reach about 9.8V (0.7V greater than the zener voltage of D55). With the unit operating normally, i.e. receiving a multiplexed analogue signal, the frequency of the Card Enable signals is such that this voltage will never be reached. When the unit is in independent mode, however (see section 8.5), VT1 remains on and C73 will charge fully, thus switching on VT13 and switching off the indicator.

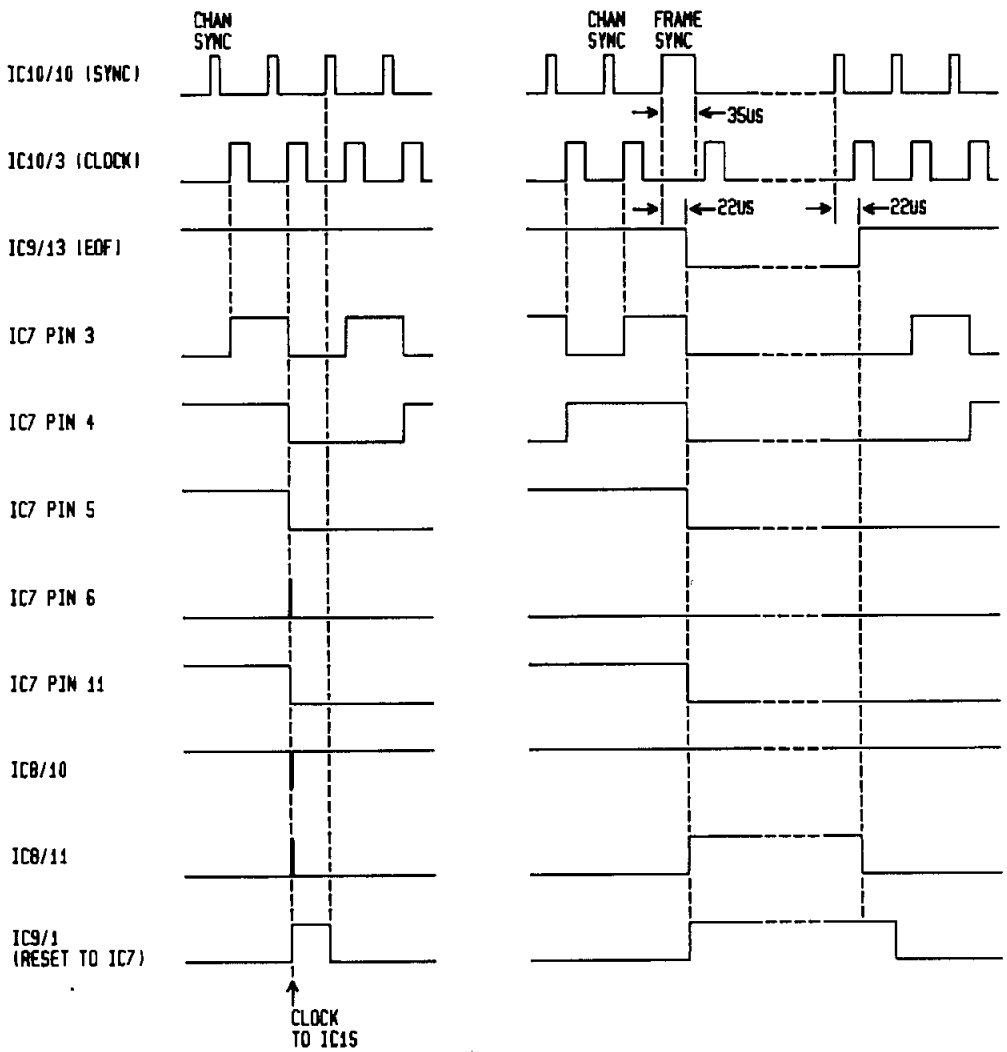
8.4 CHANNEL COUNTER

The channel counter is formed by IC7, IC8/10, IC8/11, IC9/1 and IC15 (IC16, shown forming part of the counter on the circuit diagram, is not normally fitted). It is divided into two sections. IC15 counts down from a preset value which depends on the particular group of channels served by the board, as set on the Channel Group Selector, SW1; when a count of zero is reached, a Card Enable signal is produced. The preset value is loaded by the End of Frame pulse from IC9/13.

The other half of the counter (IC7, etc.) performs a continual count from 0 to 24 at channel sync rate. Each time a count of 24 is reached, IC7 is reset and IC15 receives a clock pulse.

The two halves of IC7 are cascaded to form a five-bit counter and this receives clock pulses (on pin 1) from IC10/3 (see Fig. 8.2.2). The pins 6 and 11 outputs of IC7 (C3 and C4) are gated together in NAND gate IC8/10 so that, when a count of 24 (11000) is reached, a preset input is applied, via -NOR gate IC8/11, to bistable IC9/1. The high output produced on pin 1 of the latter resets IC7 and clocks IC15.

At the end of each channel data frame a low output appears on pin 13 of IC9/13 as described in section 8.2.5. This is routed via IC8/11 to the preset input of IC9/1 and thus holds IC7 reset until the start of the next frame as shown in Fig. 8.4.1.



CHANNEL COUNTER WAVEFORMS

FIG. 8.4.1

NOT TO SCALE

8.4.1 Card Enable

The inverted output (pin 12) of IC9/13 is applied to the preset enable (PE) input of counter IC15. When the End of Frame signal appears, the binary code produced by Channel Group Selector SW1 is loaded into the counter and this then counts down by one each time IC7 completes a count of 24 channels.

When IC15 reaches a count of zero pin 15 (=Ø) becomes high, producing the Card Enable signal described in sections 8.2.3, 8.3.1 and 8.3.3; note that IC15 will be preset to zero if the Channel Group Selector is set for channels 1-24. On receipt of the next clock pulse from IC9/1, all the counter outputs will be set high and pin 15 will go low, terminating the Card Enable signal.

8.5 INDEPENDENT OPERATION

In order that the Manual Fader Wing should continue to function in the unlikely event of an M24 Console failure, the board includes an oscillator which is enabled if no Multiplexed Input signal is being received. The channel control inputs are then multiplexed in the normal way, but the multiplexed signal is routed directly to the demultiplexer and reconverted to individual control signals.

In normal operation, the End of Frame signal from IC9/13 pin 12 triggers monostable IC5/6, the output of which has a period of Ø.5s. This is much longer than the interval between Frame Sync pulses (about 5Øms) and IC5/6 is therefore continually retriggered so that its pin 6 output remains high and pin 7 low. Under these circumstances the pin 6 output enables analogue switch IC4/4, connecting the incoming analogue multiplex to the sample-and-hold circuit (see section 8.2.2), and back-biases diode D49. At the same time the output from pin 7 inhibits gate IC1Ø/4 and analogue switch IC4/9, and enables counter IC15 (see section 8.4).

If there is no Multiplexed Input signal, there will be no sync pulses to trigger IC5/1Ø and, as a result, IC9/13 will receive no clock pulses. The End of Frame signal will not then appear and IC5/6 will not be triggered, so that pin 6 will remain low and pin 7

high (should the multiplexed input be interrupted, this state will become established when IC5/6 times-out, Ø.5s after the last EOF signal). This results in the following:

i) Analogue switch IC4/4 will be inhibited and IC4/9 enabled, connecting the multiplexed Manual Fader Wing control signals to the sample-and-hold circuit.

ii) The bases of transistors VT1 and VT2 will be pulled down via D49 and VT6, thus inhibiting the multiplex output circuit (see section 8.3.3).

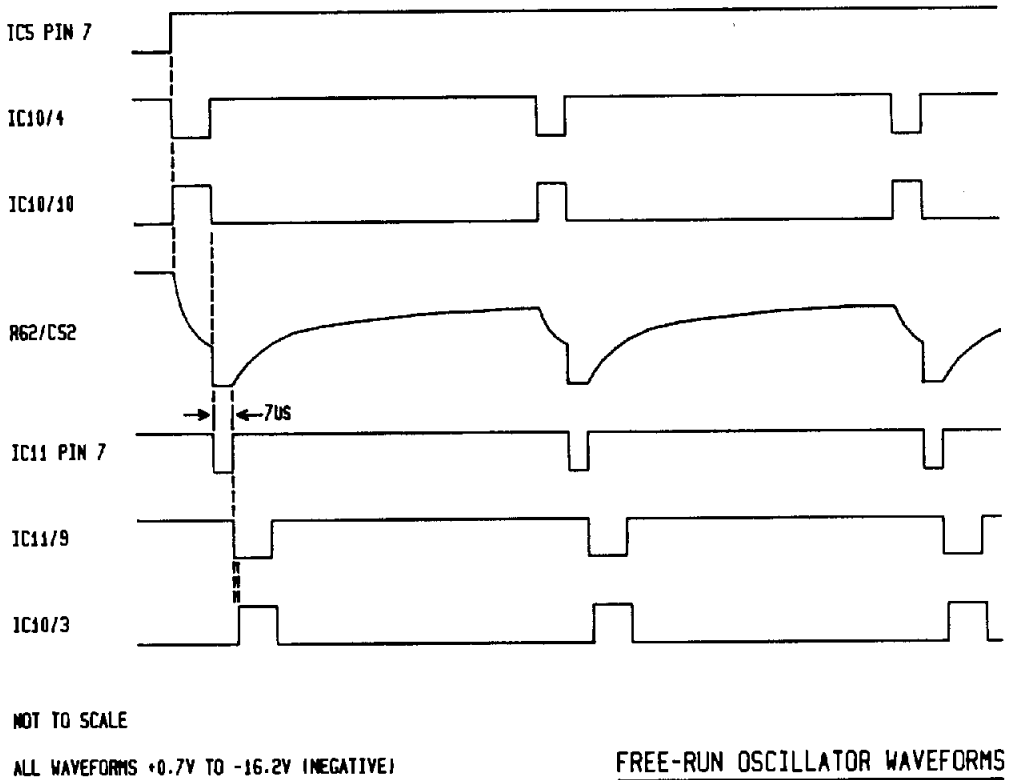
iii) A Master Reset signal will be applied to IC15, causing the outputs of this counter to be set low on receipt of the next clock pulse. This also produces a high Card Enable signal.

iv) Gate IC1Ø/4 is enabled, allowing the multiplex/demultiplex circuits to free-run.

8.5.1 Free-run Oscillator

When IC1Ø/4 is enabled by the pin 7 output of IC5/6, the initial state of the free-run oscillator depends on whether IC11/6 is or has recently been triggered. The pin 7 output of the latter monostable, when low, pulls down the junction of R62 and C52 via D51, inhibiting IC1Ø/4. When IC11 pin 7 returns high the capacitor will begin to charge via R62 and, when the threshold of Schmitt trigger IC1Ø/4 is reached, the latter will be fully enabled and will produce a low output. C52 will then discharge via R63 and D52 until the negative-going threshold of IC1Ø/4 is reached, when the output of the latter will return high.

The negative-going pulse thus produced is routed via -NOR gate IC1Ø/1Ø to the trigger input of IC11/6. The latter therefore produces a negative-going output on pin 7 and this rapidly discharges C52 via D51. When IC11/6 times-out 7us later, C52 begins to charge via R62 and the cycle repeats.



FREE-RUN OSCILLATOR WAVEFORMS

FIG. 8.5.1

Note that under these circumstances, monostable IC5/10 is triggered by the output of IC10/10, but the high output of IC3/14 prevents the appearance of the End of Frame signal. All other signals necessary for the normal functioning of the unit are generated by the free-run oscillator.

8.6 POWER-UP INHIBIT

When power is applied to the unit, capacitor C9 begins to charge via R41 and, until the threshold of IC10/11 is reached, the output of the latter will be low. This temporarily sets the unit into independent mode by clearing IC5/6 and disables the multiplexer circuit by inhibiting gate IC8/4. Once C9 has charged to the threshold of IC10/11, the latter produces a high output and the unit operates normally.

8.7 POWER SUPPLIES

The power supplies required by the board are complicated by the range of control voltage options and the limits imposed by the devices used. In particular, it is necessary to ensure that the supplies to the analogue multiplexers and demultiplexers are appropriate to the required control voltage range (i.e. positive- or negative-going), while retaining the supplies necessary for the multiplex input and output circuits, which are the same in both versions. These requirements are met as follows:

i) Positive and negative rails, VA+ and VA-, with a potential difference of 32V are generated to supply the Op-amps. These rails may be configured as +12V and -2ØV on the negative version of the board, or +2ØV and -12V on the positive version, by connecting the ØV rail via link LK4 to either the cathode or the anode respectively of a 7.5V zener diode (D16).

ii) Similarly, rails with a potential difference of 16.9V (Vdd and Vss) are generated for the CMOS logic (including the analogue multiplexers and demultiplexers). These rails may be configured as +Ø.7V and -16.2V or as +16.2V and -Ø.7V for the negative and positive versions respectively; this is achieved by linking ØV to the cathode or anode respectively of zener diode D13, using link LK3.

Note: Rails Vc+ (Ø.7V less than Vdd) and Vc- (Ø.7V greater than Vss) are used at various points in the circuit to prevent voltages at the inputs of CMOS devices exceeding the manufacturers ratings.

iii) A separate +12V rail is provided for the multiplex output circuit. This is derived from the unregulated +25V supply by means of zener diode D1.

8.7.1 Detailed Circuit Description

The incoming mains supply is applied to transformer T1, the output of which is rectified by REC1 and, after smoothing, is applied to two regulator circuits, formed by VT7, VT8 and VT9, and VT10, VT11 and VT12 respectively. Only the positive regulator will be described, the other being similar, though of the opposite polarity.

Power transistor VT9 is controlled by transistor VT8, the base of which is connected to a 13V reference produced by zener diode D17. D19, VT7 and their associated components form a constant current source for the zener diode. Feedback from the output to the emitter of VT8 provides regulation, the resulting output being about 0.7V less than the zener voltage of D17.

Zener diodes D17, D16 and D15 form a chain, by means of which the required rails for the negative and positive versions of the board are produced (D15 is the reference source for the negative regulator). On the negative version, the junction of D17 and D16 is connected to 0V via LK4, so that the positive reference is 13V and the negative reference 20.5V; this gives outputs of +12V (VA+) and -20V (VA-). On the positive version the junction of D16 and D15 is connected to 0V, thus giving a 20.5V positive reference and a 13V negative reference; the outputs are then +20V (VA+) and -12V (VA-).

The CMOS rails (Vdd and Vss) are produced by a resistor and diode chain across the outputs; this is formed by R9, D14, D13, D12 and R10. The Vc+ and Vc- rails are taken from the cathode and anode respectively of zener diode D13 (15V), while D14 and D12 provide the additional diode drops necessary to produce the Vdd and Vss rails. On the negative version of the board the junction of D14 and D13 (Vc+) is connected to 0V via link LK3, while on the positive version the junction of D13 and D12 (Vc-) is connected to 0V.

CHAPTER 9

EFFECTS PROCESSOR BOARD (Ref. 1857)

Drawing No. 6A28128 (2 Sheets)

9.1 INTRODUCTION

This board is mounted immediately behind the M24Fx control panel and is the heart of the Patch/Effects unit. It carries the panel controls and displays; a microprocessor (Effects MPU); two Peripheral Interface Adapters (PIAs); an Effects system consisting of a Chaser, a Flash Generator and a Sound-to-light Generator; and an interface with the M24 Console and the Multiplex Interface units. The program is stored in a 2Kbyte EPROM (2716-4) and a 2Kbyte RAM provides temporary and cue memory storage.

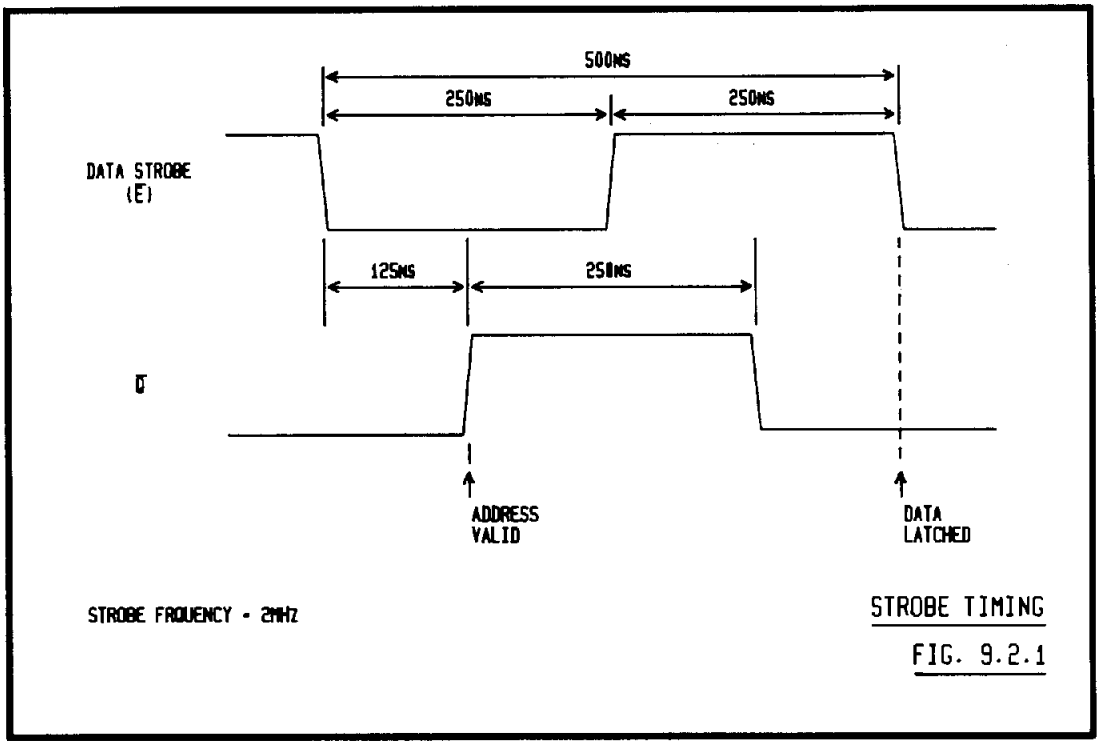
9.2 THE MICROPROCESSOR

The Effects MPU (IC9) is an MC68B09 8-bit micro-processor and this communicates with the rest of the system by means of an 8-bit Data Bus (D0 - D7) and a 16-bit Address Bus (A0 - A15). The total available address space is 64Kbytes ($0000 - $FFFF).

Correct data timing is ensured by strobe pulses 'E' and 'Q', which are derived by the MPU from an 8MHz crystal, XL1. The output of this is divided by four to give a strobe frequency of 2MHz. The timing of the 'E' and 'Q' signals is shown in Fig. 9.2.1.

9.3 EFFECTS PROCESSOR ADDRESSES

Effects MPU address lines A13 - A15 are decoded by IC10 to produce enable signals for the Program PROM ($E000 - $FFFF), the Alpha-numeric Display ($8000 - $9FFF), two Peripheral Interface Adapters ($4000 - $5FFF and $6000 - $7FFF) and Random Access Memory ($0000 - $1FFF).



STROBE TIMING

FIG. 9.2.1

9.3.1 Program PROM

The Program PROM, IC14, is a type 2716 2Kbyte EPROM located at addresses $F800 to $FFFF. The device is selected by a low output from pin 9 of decoder IC10 when A13 - A15 are all high, and its output is enabled by the low output of NAND gate IC22/6 when R/W and 'E' are both high. A third input to this gate (LDATA) is normally held high by a resistor (RN3), but may be set low to disable the PROM when using the Test Console (connected to the MC9 Test Port).

The signal from IC10 pin 9 is also used, via link LK3, to trigger monostable IC5/4. This device produces a 400ns negative-going pulse which is routed via buffer IC4/8 to the MRDY input (pin 36) of the Effects MPU, IC9. This stretches the MPU cycle to allow for the slow EPROM. If a faster (200ns) PROM is fitted, the MRDY signal may be disabled by cutting link LK3.

It should be noted that the printed circuit board has been designed to allow an 8Kbyte PROM (type 2764) to be fitted, using addresses $E000 - $FFFF, and that the pin numbers shown on the circuit diagram

apply to this device. The 2716 PROM is fitted with pin 1 in pin 3 of the dual-in-line socket.

9.3.2 Alpha-numeric Display

The keypad alpha-numeric display (DIS1) is located at addresses $8000 - $9FFF (only $8000-3 are normally used). The display is selected by a low output from pin 5 of IC10 whenever one of these addresses is accessed and a write pulse (WR) is generated by NAND gate IC22/12. The latter is enabled by 'E' and R/W except during Reset. DIS1 has four internal display registers and these are selected by A0 and A1.

9.3.3 Peripheral Interface Adapters

The two Peripheral Interface Adapters (PIAs), IC15 and IC19, are selected by the pins 3 and 4 outputs respectively of decoder IC10. The addresses concerned are $4000 - $5FFF (IC15) and $6000 - $7FFF (IC19), although only $4000-3 and $6000-3 are normally used. The registers internal to each PIA are selected by A0 and A1.

9.3.4 Random Access Memory

A type 6116LP-4 2Kbyte RAM (IC18) is located at addresses $0000 - $1FFF (only addresses $0000 - $07FF are normally used). The device is selected by a low output from pin 1 of decoder IC10, routed via transistor VT6. For MPU read actions, the RAM data outputs are enabled by the output of NAND gate IC22/6 (see section 9.3.1), while for write actions, a Write Enable pulse is produced by NAND gate IC22/12 as described in section 9.3.2.

In order to ensure that the RAM cannot become corrupted when the system is not in use, and in particular during power-up and power-down, the base of transistor VT6 is pulled down via R48 during Reset and if there is no +5V logic supply. This prevents the appearance of spurious Chip Select signals.

9.3.4.1 Battery Circuit

The contents of the eight patch memories are retained when the system is switched off by means of a battery-maintained supply provided by a rechargable nickel-cadmium battery. The battery charging circuit is formed by VT15 and its associated resistors. With the system powered-up, VT15 is switched on and current flows from the +5V rail to power the RAMs and, via resistor R98, to charge the batteries. When the power is removed, VT15 is reverse biased and the batteries supply power to the RAMs via Schottky diode D94.

9.4 PANEL INTERFACE

9.4.1 Button Matrix

The panel push-buttons and switches (with the exception of the OFF/CHASE/FLASH switches, the AUDIO 'L/R/F' switch and the momentary Flash push-buttons) are wired as a seven by six matrix with the seven rows connected to the outputs of decoder IC34 and the six columns to lines PBØ - PB5 of PIA IC15. The required output of the decoder is selected by lines PAØ - PA2 of the PIA. Each time the equipment is switched on, lines PBØ - PB5 are programmed by the MPU as inputs and PAØ - PA2 as outputs.

To detect button actions, the MPU sets each column low in turn, selecting the required output of IC34 by setting PAØ - PA2 into the appropriate states, and then reads the result via PBØ - PB5. Where a key is operated, the appropriate row will be low, while otherwise the inputs are held high via resistors (RN11). Each contact has an associated diode to prevent interaction between the rows and columns which could lead to false results when several buttons are operated at once.

The contacts are normally scanned once every 12ms in response to a 'real time' interrupt request generated by monostable IC5/5. Feedback via R13 and C9 causes this device to oscillate at the required frequency and its pin 5 output is applied to input CB1 of the PIA.

9.4.2 Indicators

Lines PAØ - PA2 of PIA IC15 are also applied to two eight-bit addressable latches, IC32 and IC33. The data inputs to these are from PIA lines PA7 and PA6 respectively, and their outputs are connected via darlington drivers (IC25 and IC26) to nine of the panel indicator LEDs (SELECT indicators A-H and the ON indicator). There are five spare outputs.

Because the address inputs to IC32 and IC33 are the same signals as are used to select the required row in the button matrix, selection of a row in the latter results in the simultaneous selection of two of the indicator latches. This makes it possible for the MPU to scan both the buttons and the indicators at the same time.

9.5 PATCH MASTER FADERS

The eight Patch Master faders, RV5 - RV12, receive a reference supply from Op-amp IC2/7, the output of which is adjustable by means of preset potentiometer RV16. The output of IC2/7 is normally set to about 5.7V to compensate for the diodes in the outputs of the faders (see below). For the same reason, the 'Ø' end of each fader is at about +Ø.2V, set by resistor R54.

The fader outputs are connected to the eight OFF/CHASE/FLASH switches. Taking Patch Master A (RV5) as an example, the switch output is routed via diode D19, while D2Ø provides an alternative route to permit Highest-takes-precedence interaction with the effects when the switch is in the CHASE or FLASH positions. A 1ØØk resistor (RN5) ensures that if the combined level is zero, the output will be ØV; this particularly necessary because of the high impedance and capacitance presented by the analogue switches in the Chase circuit when these are in the off state.

The resulting output is fed via analogue switch IC11/2, which is controlled by the PBØ line of PIA IC19 - the other Port B lines of this PIA control similar analogue switches in the other Patch master outputs. As each lighting channel is scanned, the On/Off states for that channel in the eight Patch Memories are retrieved from the RAM

and written to Port B of the PIA. The eight analogue switches are therefore each switched on or off as appropriate and, where the switch is on, the combined Patch Master and Effects level is routed to the output.

The eight analogue switch outputs are each applied to a buffer circuit - IC20/1 and its associated components in the case of Patch Master A - forming part of a Highest-takes-precedence circuit which produces the multiplexed output of the M24Fx unit. Again taking Patch Master A as an example, diode D67 performs the Highest-takes-precedence function, and diode D66 and a 47k resistor (RN7) prevent saturation of the Op-amp when D67 is back-biassed. Capacitor C20 prevents instability under these circumstances.

A ninth input to the Highest-takes-precedence circuit is the multiplexed Manual Fader Wing signal from the Multiplex Interface units. This appears on terminal 3 of connector PL3 and is routed via buffer IC29/14, which forms part of a circuit similar to that described above. The combined multiplexed output is routed to the M24 Console via a unity-gain drive circuit consisting of Op-amp IC35 and transistors VT18 and VT19.

9.5.1 Master Level Indicators

The signals at the inputs to the analogue switches are also each applied to a comparator (IC24/2 in the case of Patch master A) which drives the appropriate Master Level indicator. A potential divider formed by R136 and R137 determines the level above which the LEDs will light.

9.6 EFFECTS SYSTEM

The Effects System provides the means of generating automatic and manually controlled lighting effects such as disco lighting, flashing neon signs, lightning, etc. The system produces eight effects outputs (A - H), each of which drives the lighting channels assigned to the correspondingly labelled Patch Master fader.

The eight effects channels may each receive their input from either a Chaser or a Flash/Sound-to-light generator; three of them (F, G and H) are associated with the Sound-to-light generator, and the remainder (A - E) with the Flash generator. The effects outputs are under the control of an EFFECTS MASTER fader.

9.6.1 Effects Master Fader

The EFFECTS MASTER fader, RV4, is connected between the +5.7V reference supply and the +Ø.2V fader common. Its output is fed via a unity gain buffer formed by IC2/8 and VT7, and provides the supply for the output stages of the Chaser, the Flash Generator and the Sound-to-light Generator.

9.6.2 Chaser

The Chaser outputs are generated by the Effects MPU and appear on lines PAØ - PA7 of PIA IC19. The latter each controls an analogue switch which routes the output of the EFFECTS MASTER to the CHASE contact of the appropriate OFF/CHASE/FLASH switch.

The chase rate is determined by a variable-rate pulse generator connected to control line CA1 of PIA IC19. Op-amp IC2/1, and its associated components form a Miller integrator which produces a sawtooth waveform, the slope of which may be adjusted by means of the CHASE RATE control (RV1). This ramp is applied to the inverting input of comparator IC1/2, the output of which controls transistor VT5. With the output of IC1/2 high, VT5 is off and the output of IC2/1 rises at a rate determined by capacitor C13 and resistors R41, R42, R43 and RV1. When a level of ·5V is reached, IC1/2 changes state, switching on VT5; this causes the output of IC2/1 to fall, the slope now being primarily determined by C13 and R4Ø. The output of IC1/2 is a short, negative-going pulse, the frequency of which depends on the setting of the CHASE RATE control, and this generates an MPU interrupt request via the CA1 line of the PIA.

9.6.3 Flash Generator

The Flash Generator is formed by IC2/14 and IC1/1 and their associated components. It is similar to the chase rate generator described in the previous section, but in this case the output is taken from the Miller integrator (IC2/14). Comparators IC1/14 and IC1/13 compare the ramp with the setting of the MARK-SPACE control (RV2), respectively producing inverted and non-inverted flash signals. These are applied to the FLASH contacts of the OFF/CHASE/FLASH switches associated with Patch Masters B and D (inverted) and A, C and E (non-inverted).

9.6.4 Sound-to-light Generator

The Sound-to-light generator is associated with Patch Masters F (treble), G (middle) and H (bass) and is selected when any of the corresponding OFF/CHASE/FLASH switches are in the FLASH position. The audio input appears on terminals 3 (left) and 5 (right) of connector SK1 and either channel or a random flicker signal may be selected by means of the 'L/R/F' switch, SW41.

The input signal is applied to pin 13 of amplifier IC3/14, the output of which is a.c. coupled, via capacitor C38, to pin 9 of a second amplifier, IC3/8. The output of the latter is applied to the three filter circuits and also to IC3/7, which detects the peaks of the amplified signal and, via zener diode D86, controls the input level by means of FET VT9. Diode D87 determines the level at which the FET switches on.

The output from IC3/8 is applied to the three sensitivity controls; RV15 (treble), RV14 (middle) and RV13 (bass). Each of these is connected at the input of a filter circuit which covers the appropriate range of frequencies, i.e. above 2.5kHz, 120-2500Hz and below 120Hz respectively.

Taking the treble filter as an example, the filter is formed by Op-amp IC13/8 and its associated components and its output is applied to a second Op-amp, IC13/7. The output of the latter is routed via diode D88 to capacitor C45, which stores the positive

peaks of the filtered waveform. The resulting signal drives transistor VT11 which switches the output of the EFFECTS MASTER onto the Sound-to-light contact of OFF/CHASE/FLASH switch SW17.

9.6.4.1 Random Flicker

Schmitt triggers IC37 and their associated components form four oscillators with different frequencies, the outputs of which interact to give, on the output of IC37/4, a signal which flashes randomly. This is a.c. coupled via C37 to amplifier IC3/1 and the output of the latter is connected to the 'F' contact of switch SW41.

9.6.5 Flash Buttons

The outputs from the eight OFF/CHASE/FLASH switches (for example, at the cathodes of diodes D19 and D2Ø in the case of Patch Master A) may be connected directly to the fader reference voltage by means of momentary action 'Flash' buttons (e.g. SW42). If required, link LK2 may be moved to position B/C to allow the assigned channels to be switched to the current EFFECTS MASTER level.

9.7 SYNC DETECTOR

In addition to providing patch and effects facilities, etc. M24Fx can act as a back-up to M24, thus permitting continued operation in the unlikely event of failure of the main console.

In normal operation, the multiplexed Manual Fader Wing signals from the Multiplex Interface units are combined on a highest-takes-precedence basis with the output of M24Fx and routed to the M24 Console, while the output from the M24 Console is routed to the Multiplex Interface units via M24Fx without additional processing. The timing of the operation is controlled by the sync pulses from M24.

If for any reason the sync pulses from the M24 Console cease, a relay will change over, routing the combined Manual Fader Wing and M24Fx signals to the Multiplex Interface units, and M24Fx will generate sync pulses. These sync pulses will be superimposed on the

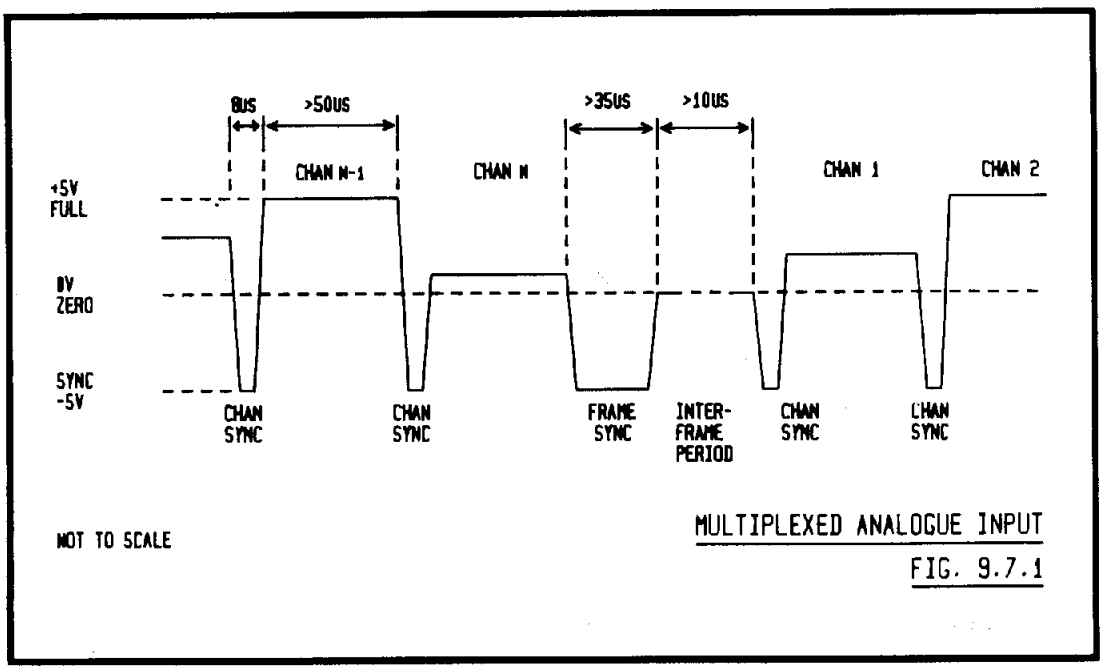
multiplexed analogue output or transmitted separately, depending on whether the system in use is two-wire or four-wire.

9.7.1 Normal Operation

The multiplexed analogue signal from M24 appears on terminal 4 of connector PL2 and, terminated by capacitor C31 and resistors R18 and R19, is applied to unity-gain buffer IC29/1. The signal takes the form shown in Fig. 9.7.1. The analogue channel level varies between +5V (full level) and 0V (zero), while the sync pulses are negative-going to -5V.

Note: Some equipment may use an alternative, four-wire system which has separate analogue and sync signals. In the latter case, the sync signals appear on terminals 5 and 6 of PL2 and are applied to Op-amp IC29/7 which acts as a differential line receiver.

The output of IC29/1 is applied, via diode D12, to IC29/7 which, in the case of the two-wire system, acts as a simple inverting amplifier with a gain of 2. The diode provides isolation from the analogue signals when using the four wire system.



MULTIPLEXED ANALOGUE INPUT
FIG. 9.7.1

The output of IC29/7 is routed via a third Op-amp, IC29/8, which has positive feedback via R147, giving a Schmitt trigger action. The output of the latter is applied, via capacitor C58 and buffers IC37/1 and IC37/12, to bistable IC30/1 and monostables IC28/7, IC28/10 and IC27/9. C58 provides a.c. coupling, thus allowing the signal to be converted to the voltage levels required by the CMOS logic; diode D96 ensures that the permissible input levels are not exceeded.

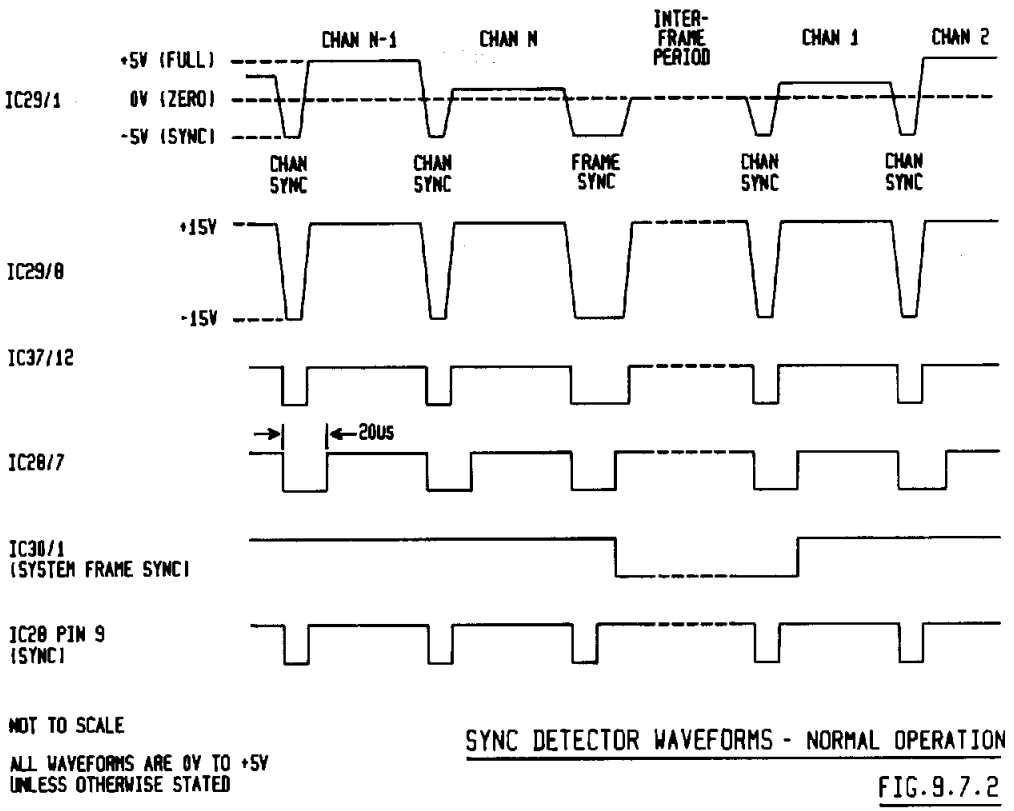
9.7.1.1 Frame Sync Separator

At the end of each frame of channel level data, a frame sync pulse with a duration of at least 35us appears on the multiplexed analogue input. This is detected by means of monostable IC28/7 (20us), which is triggered on the leading edge of every sync pulse by the output of IC37/12. The output from pin 7 of IC28/7 is applied to the clock input of bistable IC30/1, the D input to which (pin 5) is the sync signal from IC37/12. On the trailing edge of the 20us pulse from IC28/7, IC30/1 is clocked and its pin 1 output is set low or high, depending on the state of its D input. In the case of the Channel Sync pulses, IC37/1 returns high after 8us and IC30 pin 1 is set high. When the longer Frame Sync pulse appears, however, IC37/12 is still low after 20us and pin 1 of IC30 is set low.

The System Frame Sync signal thus produced is used to generate an MPU interrupt request via line CA1 of PIA IC15. In addition, the pin 2 output of IC30/1 clocks a second bistable, IC30/13 (see next section).

9.7.1.2 Multiplex Detector

Monostable IC27/9 has a period of 0.5s and is continually retriggered by the M24 sync pulses from IC37/12. Its low pin 9 output is applied to the D input of bistable IC30/13, which is clocked by the inverted System Frame Sync pulse from pin 2 of IC30/1. The output of IC30/13 has three functions:



SYNC DETECTOR WAVEFORMS - NORMAL OPERATION

FIG.9.7.2

i) It pulls down the pin 12 input of monostable IC28/10 via diode D82. This allows the monostable to be triggered by the sync pulses from IC37/12, but prevents triggering by IC27/9 (see section 9.7.2).

ii) It inhibits NAND gate IC22/8, thus preventing the pulses from IC28/10 appearing on the multiplexed output.

iii) It turns transistor VT14 off, thus de-energising relay RL and making the following connections:

RL/1 Connects the multiplex input from M24 to terminal 2 of connector PL3 (output to Multiplex Interface units, two-wire).

RL/2 Connects the multiplex input from M24 to terminal 2 of connector PL4 (output to Multiplex Interface units, four-wire).

RL/3, RL/4 Connect the four-wire sync signals from M24 to terminals 3 and 4 of connector PL4 (sync to Multiplex Interface units).

9.7.1.3 Sync Interrupt

The M24 sync signals from IC37/12 also trigger monostable IC28/1Ø (enabled by IC3Ø/13 via diode D82) and the 8us negative-going pulse produced on pin 9 of this device is applied to line CB1 of PIA IC19. This generates a Fast Interrupt Request (FIRQ), in response to which the MPU retrieves the On/Off states for the next channel from the Patch Memories in the RAM, and writes these to Port B of IC19 as described in section 9.5.

9.7.2 Operation in Back-up Mode

If for any reason the M24 Console is inoperative or not connected, M24Fx will generate the sync pulses necessary to ensure correct operation. The absence of M24 sync pulses means that IC27/9 pin 9 will be high, presetting bistable IC3Ø/13. The latter therefore produces a high output on pin 13 which has the following effects:

i) Diode D82 is back biassed, thus allowing IC27/7 to clock IC28/1Ø.

ii) NAND gate IC22/8 is enabled, thus allowing the pulses from IC28/1Ø to appear on the multiplexed output - see section 9.7.2.1.

iii) Relay RL is energised via transistor VT14, thus making the following connections:

RL/1 Connects the output of the line driver (see section 9.5) to terminal 2 of connector PL3 (output to Multiplex Interface units, two-wire).

RL/2 Connects the output of the line driver to terminal 2 of connector PL4 (output to Multiplex Interface units, four-wire).

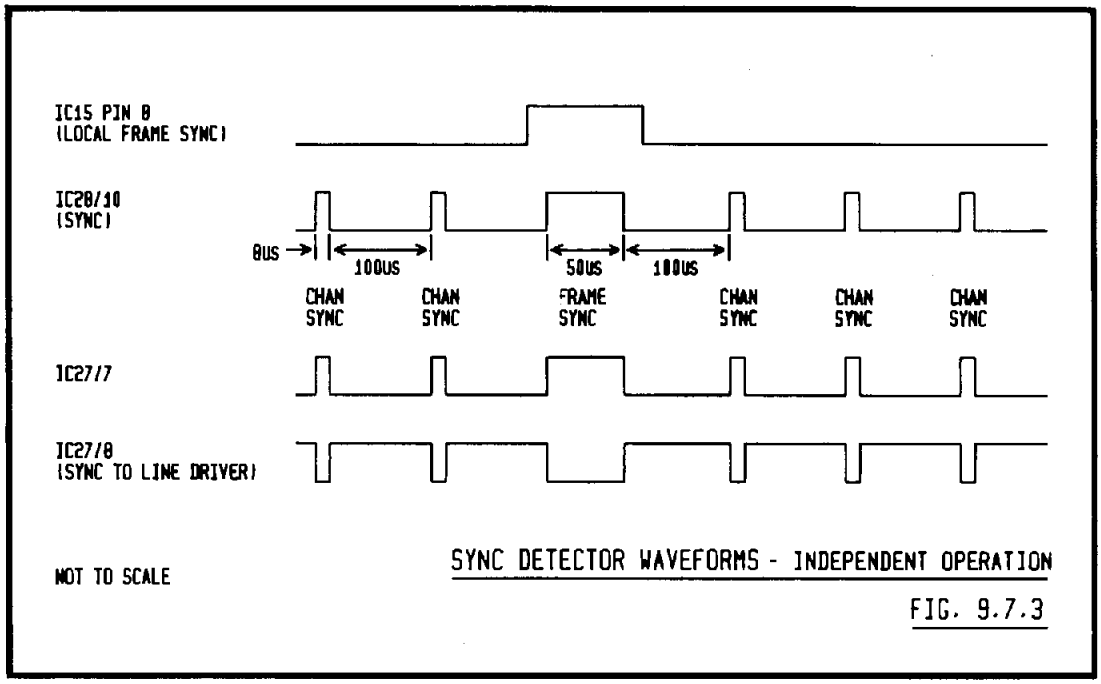
RL/3, RL/4 Connect the four-wire sync signals from differential line driver IC31 to terminals 3 and 4 of connector PL4 (sync to Multiplex Interface units). See section 9.7.2.1.

9.7.2.1 Sync Generator

Monostables IC28/10 and IC27/7 together form an oscillator which, when enabled by a high output from pin 13 of IC30, produces an 8us positive-going sync pulse on pin 10 of IC28 about every 108us. These pulses are routed via NAND gate IC22/8 (enabled by IC30/13) to differential line driver IC31 (four-wire) and transistor VT17. On two-wire systems, VT17 controls a second transistor, VT16, which connects the input of IC35 to -5V (produced from the -15V rail by zener diode D37); this superimposes negative-going sync pulses on the analogue multiplex produced by the Highest-takes-precedence circuit (see section 9.5). In the case of the four-wire system, terminal 4 of connector PL3 is connected to 0V, thus preventing VT17 turning on and ensuring that VT16 remains off.

9.7.2.2 Local Frame Sync

The time constant of IC27/10 (8us) is normally determined by capacitor C26 and resistors R80, R81 and R93, transistor VT13 being switched on by a low output from line PA6 of PIA IC15. When the last channel in the frame (channel sixty) has been processed, the MPU sets line PA6 of PIA IC15 (Local Frame Sync) high. This switches off transistor VT13, increasing the time constant of monostable IC27/10 to about 50us (determined by C26 and R80). A Frame Sync pulse is thus generated at the output when IC27/10 is next triggered. At the end of this extended pulse (detected via line PA5 of PIA IC15), the MPU returns PA6 to its normal low state and then starts the next frame.



SYNC DETECTOR WAVEFORMS - INDEPENDENT OPERATION

FIG. 9.7.3

9.7.2.3 Entering Back-up Mode

If the sync pulses from the M24 Console stop during normal operation, there will be a 0.5s pause before IC27/9 times-out and M24Fx takes over. At the end of this pause, IC30/13 will be preset, enabling IC22/8, energising relay RL and enabling the oscillator formed by IC27/10 and IC28/7. When the relay is energised, the sync pulses from IC27/10 and the output of the analogue line driver, will be connected to the Multiplex Interface units. The frame will then continue from the channel it had reached under M24 control, the sync pulses now being generated by IC27/10, triggered by IC28/7.

When sixty channels have been processed, the MPU generates a Frame Sync pulse as described in the previous section and then starts a new frame. Note that although the M24 Console may not be controlling as many as sixty channels, when in Back-up Mode M24Fx always generates a frame of this size).

9.7.2.4 Returning to Normal Mode

If sync pulses generated by the M24 Console start to appear when M24Fx is operating in back-up mode, there will be an indeterminate period of up to 100ms during which neither system has full control.

The first sync pulse from M24 triggers IC27/9, thus removing the preset input to IC3Ø/13 and setting the D input (pin 9) of this bistable low. IC28/7 is also triggered and this clocks IC3Ø/1 so that, on the first frame sync, pin 2 of the latter will be set high, clocking IC3Ø/13. This inhibits IC22/8, de-energises relay RL and disables the sync oscillator (IC28/1Ø and IC27/7). This first frame sync pulse also interrupts the MPU via line CA1 of PIA IC15 and normal operation, as described in section 9.7.1, commences.

9.8 CHANNEL 'ON' DETECTOR

In order that the output levels of the lighting channels may be determined for use when the LOAD OUTPUT button is operated, the multiplexed analogue output to the Multiplex Interface units (connector PL3 terminal 2) is applied to comparator IC8. The other input to this device is held at about Ø.9V by potential divider R62/R63 and its output is connected to line PA7 of PIA IC15.

9.8 RESET CIRCUIT

The reset circuit is formed by transistors VT1 - VT4, and their associated components. The circuit has two functions: firstly, to generate a reset pulse each time the equipment is switched on, thus ensuring that the MPU enters its start-up procedure correctly, and secondly, to inhibit processor operation if the voltages on the +5V and +15V rails vary by more than the allowed tolerance.

As the +5V rail becomes established at switch on, the voltage at the junction of C1, R11 and D2 will rise rapidly and VT3 will switch on. This pulls the Reset line low, lighting LED D22. When the rail reaches +3.6V, the voltage on the base of VT3 falls below Ø.7V, and this transistor switches off. The Reset line is then pulled high by resistor R1.

In normal operation, the emitter of transistor VT1 is close to the +5V rail and the base of VT2 at about 1V; the latter transistor is therefore on and VT4 off. If either rail starts to fall, the voltage on the base of VT2 will also fall until VT2 switches off; VT4 will then switch on, pulling down the Reset line. In addition,

the MPU may be reset by means of a manual reset switch, SW1, which pulls down the base of VT2.

The Reset signal is routed to the MPU (IC9), both PIAs (IC15 and IC19), the indicator latches (IC32 and IC33), the alpha-numeric display (DIS1) and the real-time interrupt generator (IC5/5). In addition, it inhibits NAND gate IC22/12 and pulls down the base of transistor VT6 (via diodes D65 and D64) to ensure that no spurious RAM Write Enable or Chip Select signals are generated.

CHAPTER 10

SERVICING AND MAINTENANCE

10.1 INTRODUCTION

This chapter provides details for the initial setting-up of the equipment, routine maintenance, power checks and the methods for removal and insertion of modules, components etc.

10.1.1 Equipment Required

The following equipment is required in order to maintain the system:

i) Multi-meter

The Multi-meter should have the following ranges and accuracy:

0 to 5V d.c.	(1%)
0 to 15V d.c.	(1%)
0 to 40V a.c.	(2%)
0 to 110/240V a.c.	(5%)
0 to 10mA	(10%)
0 to 10A	(5%)

ii) Oscilloscope

The oscilloscope should be a dual-trace type capable of measuring signals of:

0 to 15V d.c.
0 to 110/240V a.c.
Time-base switching <10ns to >3 secs.

iii) Solder Remover

This should be of the 'suction' type.

iv) Soldering Iron

This should be of a temperature-controlled type, with a maximum temperature not greater than 370 degrees Celsius.

10.1.2 General Cautions

10.1.2.1 Power

The System is powered from either a 110V or a 240V a.c. source. **THIS VOLTAGE CAN BE FATAL.** Whenever the power terminals are exposed, the technician should be insulated from ground (preferably using a rubber mat). Always disconnect the equipment from the mains when removing or refitting sub-assemblies, only restoring the power when it is essential to work with the system 'live'.

10.1.2.2 Proms

Erasable Programmable Read Only Memories (as used on the Motherboard and the Panel board) must not be exposed to direct sunlight or to ultra-violet light. Continuous exposure may destroy the program content.

10.1.2.3 Printed Circuit Boards

Care must be exercised when removing or inserting the Printed Circuit Boards to ensure that they do not bend, as this could cause cracking of the circuit tracks. Never force a board into place.

10.1.2.4 Handling CMOS Integrated Circuits

CMOS DEVICES ARE DESTROYED BY STATIC ELECTRICITY. When handling these integrated circuits, ensure that YOU and THE BENCH are at the same potential. Failure to do so could result in damage to the IC. A convenient method of achieving this is to use a copper ring which fits one finger and arrange a flexible wire which incorporates a 1M0 resistor from the ring to the bench, the surface of which should be earthed metal. **THIS PROCEDURE MUST NOT BE ADOPTED WHEN THERE ARE HAZARDOUS VOLTAGES PRESENT.**

Always ensure that integrated circuits remain in their wrapping until you need them - never leave them un-earthed (the wrapping 'earths' all the pins, avoiding capacitatively induced voltage). Under no circumstances should such devices be stored in polythene or other high static containers.

10.1.2.5 Food and Drink

Food or drink should not be consumed in the immediate vicinity of the equipment. Drinks, especially those containing sugar, could cause irreparable damage, apart from the possibility of short-circuiting the power supplies.

10.1.2.6 Control Panels

The appearance of the system may be damaged by direct contact with excessive heat such as a soldering iron or a cigarette. Care should be exercised.

10.2 INITIAL SETTING-UP

The system is supplied configured to the requirements envisaged at the time of purchase. However, circumstances may demand expansion of the system or the addition of optional facilities.

Variation of the system parameters may be achieved by altering patch links or by changing the settings of Dual-in-Line switches located on the Motherboard. The Motherboard also carries preset potentiometers which may require adjustment when a replacement board is fitted. Note that links must be set BEFORE the boards are inserted.

Configuration and adjustment procedures are detailed below for each board.

WARNING: Removing the cover from any unit exposes connections at mains voltage. Any measurements or adjustments which require the system to be 'live' should only be carried out by qualified electricians familiar with this type of equipment.

10.2.1 Panel Board (Ref. 1833)

There are no links or configuration switches on the Panel board which require setting-up before the equipment is used. It should be noted, however, that the printed circuit board has been designed to allow an 8Kbyte PROM (type 2764) to be fitted and that the pin numbers shown on the circuit diagram apply to this device. The 2716 PROM usually provided is fitted with pin 1 in pin 3 of the dual-in-line socket.

10.2.2 Motherboard (Ref. 1832)

Before inserting a replacement board, check that the following links are in the correct positions:

LK1, LK2	-	Not fitted in this application.
LK3 to LK5	-	PROM Delay links. Normally fitted. May be removed if the board has 200ns PROMs.
LK6	-	Normally fitted in position A/B.
LK7	-	Not fitted in this application.
LK8	-	Normally fitted in position A/C.
LK9	-	Not fitted in this application.

When the board has been installed, the analogue interface must be set-up as follows:

i) Monitor terminal 2 of connector PL4 (O/P DMX) on the Motherboard, with reference to terminal 1 (ØV), using an oscilloscope triggered from pin 39 of PIA IC21 (Frame Sync).

ii) Select channel 1 and set it to maximum level, ensuring that the Memory master fader is also at full. Adjust potentiometer RV2 until the analogue signal for the channel is at +5V.

iii) Set channel 1 on the Manual Fader Wing to full, ensuring that any master faders are also at full. Set the Memory master on the M24 Console to zero and the Manual master to full.

iv) Adjust potentiometer RV1 until the Video Mimic just displays 'F' for channel 1. Check the adjustment by lowering the Manual master fader and then returning it to full.

Alternatively, the following method may be used if no Video Mimic is provided:

i) Disconnect the dimmer drive outputs from the Multiplex Interface unit serving channels 1-24. Remove the cover from the unit and monitor the multiplexed analogue signal on test point TP5, with reference to TP6 (ØV), using an accurate oscilloscope. Trigger the oscilloscope from test point TP2 (EOF).

ii) Switch off the M24 Control Console, and set channel 1 on the Manual Fader Wing to full, ensuring that any master faders are also at full. Note the multiplexed analogue voltage for this channel.

iii) Switch on the M24 Control Console and set the Manual master fader to zero and the Memory master fader to full. Set channel 1 to full.

iv) Adjust RV2 on the console Motherboard to obtain the same multiplexed analogue voltage for channel 1 as before. This may be checked by switching the Control Console off and on.

v) Set the Memory master fader on the Control Console to zero and the Manual master fader to full. Adjust RV1 on the console Motherboard to obtain the same multiplexed analogue voltage as before. This may be checked by lowering each master fader in turn and adjusting the preset control so that there is no change.

10.2.3 Wheel Interface Board (Ref. 1706)

This board cannot be set-up until the wheel is fully assembled.

Using an oscilloscope set to 100mV per division and timebase set to 0.1ms per division, monitor TP1A, with reference to TP3. Rotate the wheel slowly until the minimum voltage is found. As the wheel is rotated, the voltage should switch between 'black' and 'white' levels; if the voltage remains constant over any part of the travel, adjust RV1 until the voltage is approximately 400mV and then relocate the minimum voltage point. This minimum voltage ('black' level) should be between 200mV and 300mV. Moving the wheel slightly should cause a change to approximately 600mV.

Monitor TP1, using a voltage range of 2V per division and a timebase of 5ms per division. Rotate the wheel at a constant rate and adjust RV1 slightly until a 1:1 mark-space ratio is obtained.

Repeat the procedure for the second sensor, monitoring TP2A and TP2, and adjusting RV2.

Examine TP1 and TP2 simultaneously; the two signals should be 90° out of phase as shown in the diagram (Fig. 4.2.1) in Chapter 4.

10.2.4 Video Interface (Ref. 1834)

Before inserting a replacement board, check that the Board Address Select links (LK1 to LK6) are fitted as follows:

LK1 - LK3, LK6 : Fitted.
LK4, LK5 : Not fitted.

} Addresses $1808 - $180B

1Ø.2.5 Console and M24Fx Power Supply Units

The only adjustments which may be carried out on the Power supply units are to select the required mains voltage, as shown on the circuit diagrams (Drawings Nos. 7C26933 and 7C28189), and to choose a replacement for resistor R11. The latter component is selected when the equipment is tested and will only need replacement if the output tolerance of the +5V supply is exceeded (see Drawings Nos. 6C26865 and 6C28178).

1Ø.2.6 Multiplex/Demultiplex Board (Ref. 1828)

Before a replacement board is fitted, links LK1, LK2, LK3 and LK4 must be checked to ensure that they are in the same positions as those on the board removed. LK5 is not normally fitted. The links are set during manufacture to conform with positive or negative dimmer control signals. It is not recommended that these are changed subsequently, as diodes D23 to D46 must be reversed to change the polarity of the signal and R92 to R115 must be replaced with resistors of the correct value (usually 1Øk Ø for negative control signals or 1kØ for positive). In addition, capacitor C5 is omitted for negative control signals and C6 for positive.

Note: All four links must be in either the '-ve' or the '+ve' position. If some are in one position and some in the other severe damage will result.

Other possible adjustments are as follows:

i) Input and output control voltage ranges, i.e. -5V, -1ØV or -15V (negative), or +5V, +1ØV or +15V (positive). This is done by selecting the appropriate values for resistors R48 and R23, as given in the table on Drawing No. 6A26850. Both the input and the output range must be the same.

ii) Mains input voltage. This is changed by rewiring the mains input terminals on the printed circuit board (see Drawing No. 7B26872).

It is not possible to convert a Tempus/Bleecon type unit to a D-connector type or vice versa.

10.2.7 Effects Processor Board (Ref. 1857)

Before inserting a replacement board, check that the following links are in the correct positions:

LK1 - Normally fitted in position A/C.

LK2 - Normally fitted in position A/B (see section [G].6.5).

LK3 - PROM Delay link. Normally fitted. May be removed if the board has a 200ns PROM.

It should be noted that the printed circuit board has been designed to allow an 8Kbyte PROM (type 2764) to be fitted and that the pin numbers shown on the circuit diagram apply to this device. The 2716 PROM usually provided is fitted with pin 1 in pin 3 of the dual-in-line socket.

When the board has been installed and the unit reassembled, it may be necessary to set-up the Fader Reference. There are two ways of doing this, but the first method may only be used if a Video Mimic is provided:

i) Set the Manual master fader on the M24 Control Console to full and the Memory master to zero. Select channel 1 on M24Fx and set it On in any of the eight Patch Master memories. Set the corresponding master fader to full and the others to zero, ensuring that all the OFF/CHASE/FLASH switches are set to OFF.

ii) With M24Fx standing on its lid, remove the three screws nearest the wide end of the left-hand end plate, slackening the remaining screw. The end plate will then hinge down, exposing the end of the Effects Processor board. The Fader Reference potentiometer (RV16) is near the wide end of the unit next to the red Reset button.

iii) Adjust RV16 until the Video Mimic just displays 'F' for channel 1. Check the adjustment by lowering the Patch Master fader and operating the corresponding momentary Flash button and then returning the fader to full.

If, however, M24 is not provided with a Video Mimic, the following method should be used.

i) Disconnect the dimmer drive outputs from the Multiplex Interface unit serving channels 1-24. Remove the cover from the unit and monitor the multiplexed analogue signal on test point TP5, with reference to TP6 (ØV), using an accurate oscilloscope. Trigger the oscilloscope from test point TP2 (EOF).

ii) Set the Manual master fader on the M24 Control Console to zero and the Memory master fader to full. Set channel 1 to full and note the multiplexed analogue voltage for this channel.

iii) Set the Manual master fader on the M24 Control Console to full and the Memory master to zero. Select channel 1 on M24Fx and set it On in any of the eight Patch Master memories. Set the corresponding master fader to full and the others to zero, ensuring that all the OFF/CHASE/FLASH switches are set to OFF.

iv) Adjust RV16 on the M24Fx Effects Processor board to obtain the same multiplexed analogue voltage for channel 1 as before. This may be checked by lowering each master fader on the M24 Console in turn and adjusting RV16 on M24Fx so that there is no change.

1Ø.3 ROUTINE SERVICING

The following routine is recommended in order to maintain the equipment in working order. The indicated servicing intervals are given as a general guide and should be increased or decreased according to how much the equipment is used.

10.3.1 Weekly

Clean, using a lint-free anti-static cloth, the outer surfaces of the M24 and M24Fx Control Consoles, the Video Mimic (including the screen), the Multiplex Interface Units and the Manual Fader Wing.

If a persistent mark cannot be removed this way, the use of a SMALL AMOUNT of antistatic cleaner is recommended. Do not use any other type of cleaner as scratching, discoloration and loss of the non-reflecting surface quality may result. Under no circumstances should spray polishes be used near the panels as they may destroy the slider faders.

10.3.2 Quarterly

Carry out the Weekly cleaning and check the following:

i) Security of interconnecting plugs and sockets.

ii) Cable insulation - replace damaged cables immediately.

iii) Run the Test Programs to ensure that all facilities are functioning correctly.

10.3.3 Yearly

Carry out the Weekly/Quarterly maintenance and, in addition clean the resistive surfaces of the M24 Control Console fade duration controls. Access to these is obtained as follows:

i) Switch off the mains supply to the console and unplug any cables which are connected.

ii) Carefully lever off the plastic fader knobs. Then fit the plastic lid to the console to protect the front panel controls and turn it over so that the bottom cover is facing upwards.

iii) Remove the bottom cover, the Video Interface board, the Video Output panel, the Motherboard and the Panel board as described in section 1Ø.5.1.

The Fade Duration controls may now be cleaned using a lightly dampened cloth (water only). Then run the slider over the surfaces several times, wiping away any dirt accumulations. Ensure that the surfaces are dry before reassembling the console.

Notes: 1) Do not use anything but pure water as irreparable damage to the slider surfaces could result.

2) The Master Faders and the M24Fx Patch Master Faders are sealed and will not require cleaning.

1Ø.4 POWER SUPPLIES

WARNING: Connections at mains voltage are exposed if the cover is removed from any unit. Any measurements or adjustments which require the system to be 'live' should only be carried out by qualified electricians familiar with this type of equipment.

The M24 Console and M24Fx Power Supply units are fully described in Chapter 6. No adjustments are possible, but in the event of a fault the output voltages should be checked, measuring these at the multi-pin connector on the appropriate unit, with the system in operation - see Drawings Nos. 7C26933 (M24) and 7C28189 (M24Fx). All voltages should be measured with respect to the ØV terminals on this connector.

There are also no adjustments possible on the Multiplex Interface unit. The supply voltages may be checked, however, at various points on the printed circuit board (see circuit diagram - Drawing No. 6A26850). Always measure with respect to test point TP6 (ØV).

10.4.2 Fuses

10.4.2.1 Control Console

The mains input to the Control Console is protected by a 2A HRC fuse (3.15A on 110V-120V versions) mounted on the rear of the bottom cover, adjacent to the mains input plug. The only other fuses in the Console are on the Power Supply board; these are quick-blow type rated at 5A and are accessible after removing the bottom cover (see section 10.5.1.1).

10.4.2.2 Multiplex Interface Unit

The mains input to the Multiplex Interface unit is protected by 100mA quick-blow fuse mounted in a holder which forms part of the chassis mounted mains input plug. The holder should be carefully levered out using a small screwdriver or other suitable implement.

10.4.2.3 M24Fx

The mains input to the M24Fx unit is protected by a 2A HRC fuse (3.15A on 110-120V versions) mounted on the connector panel in the rear extrusion, adjacent to the mains input plug. The only other fuses in the unit are on the Power Supply board; these are quick-blow type rated at 5A and are accessible after removing the bottom cover (see section 10.5.3.1).

10.5 REMOVAL AND REFITTING OF SUB-ASSEMBLIES

The following details the removal and replacement of the various parts of the system.

WARNING: Connections at mains voltage are exposed if the cover is removed from any unit. Disconnect the system from the mains before commencing work. Apart from the dangers of electricity at mains voltage, components could be damaged if removed or fitted with the system in operation.

1Ø.5.1 Control Console

1Ø.5.1.1 Preliminary

i) Before removing any part of the console all cables should be disconnected and the plastic lid fitted. If the Panel board is to be removed, the fader knobs must be carefully levered off before fitting the lid.

ii) Turn the console over so that the bottom is facing upwards and the rear extrusion towards you.

iii) Using a 'Posidrive' No 1 screwdriver, remove the eight screws around the edge of the bottom cover and lift it away to one side.

iv) The power supply chassis is fitted to the cover and connected to the Motherboard by a cable assembly. The cable assembly and the earth bond (the separate green/yellow wire) should be unplugged from the power supply unit. When removing the earth bond, do not pull the wire; the connector is of a special type which can only be removed by pulling the plastic shroud.

1Ø.5.1.2 Power Supply Unit

The Power Supply unit is fitted inside the bottom cover of the console and secured by six screws. Complete replacement units are available from Rank Strand.

1Ø.5.1.3 Video Interface

The Video Interface board is connected to one of the five multipin connectors at the right hand end of the Motherboard and is secured by a screw passing through a small bracket at the wide end of the board and a plastic retaining clip at the narrow end. Remove the board carefully, taking care not to damage the wiring to the Modulator board. Finally remove the output connector.

The Video Output panel may now be removed from the rear extrusion; it is secured by two screws. Take care not to damage components on the Modulator board or the Motherboard.

Replacement is the reverse of removal, but the following should be noted:

i) When replacing the Video Output panel take care not to damage components on the Modulator board or the Motherboard. Note that the bottom edge of the panel (i.e. the uppermost edge with the console inverted) engages in a slot in the rear extrusion.

ii) Ensure that the output connector is replaced correctly. The socket marked '1' mates with the terminal nearest the edge of the Video Interface board.

iii) Ensure that the narrow end of the Video Interface board engages in the plastic retaining clip.

10.5.1.4 Motherboard

i) Remove the bottom cover of the console, the Video Interface board and the Video Output panel as described in the preceding sections. It is not essential that the Video Output panel be removed, but removing the Motherboard is easier if this is done.

ii) Disconnect the multiplex, tape and Panel board connectors from the Motherboard.

iii) Release the six clips securing the Motherboard to the Panel board and lift the board off the supporting pillars.

Replacement is the reverse of the above, but the following must be noted:

i) Ensure that all connectors are replaced correctly. The Panel board connector has small arrows on both plug and socket to indicate terminal 1.

ii) The cable from the Multiplex Output connector on the rear of the console connects to the plug marked 'PL4' on the Motherboard (the adjacent connector marked 'PL3' is only used on equipment using the four wire multiplex system).

iii) Lay the cables so that they will not be damaged or sandwiched between the two boards when the bottom cover is replaced.

10.5.1.5 Panel Board

i) Remove the bottom cover of the console, the Video Interface board and the Video Output panel as described in the preceding sections. The Motherboard may also be removed if required, or alternatively the Panel board and Motherboard may be removed as a complete assembly.

ii) Disconnect the REC LOCK keyswitch and channel control wheel connectors from the Panel board. Disconnect the multiplex and tape connectors from the Motherboard if this has not already been done. Remove the Multiplex/Tape panel from the rear extrusion.

iii) Remove the six screws holding the Panel board in place. Note that five of these are fitted with clear spacers to ensure that the screw heads are readily accessible with the Motherboard in position. Lift the Panel board out of the console.

Replacement is the reverse of the above. Ensure that the ribbon cable from the channel control wheel does not prevent free movement of the wheel.

10.5.1.6 Channel Control Wheel

Disconnect the ribbon cable from the connector on the Panel board. Use an M3 nut runner to remove the two nuts holding the wheel assembly in place. The complete wheel assembly is available as a spare from Rank Strand and their agents.

10.5.2 Multiplex Interface Unit

With the exception of the mains input connector, the multiplex connectors and, on the Tempus type unit, the Manual Fader Wing input connectors and the dimmer drive output cables, all the components of the Multiplex Interface unit are assembled on a single printed circuit board.

The board is accessible after removing the top half of the unit (secured by four screws) and, if required, disconnecting the earth bond from this cover. **DISCONNECT THE UNIT FROM THE MAINS BEFORE REMOVING THE COVER.**

The board is held in place by six screws (eight on units with 'D' connectors). First disconnect the front panel 'molex' connectors, taking careful note of their positions to ensure correct replacement. Then remove the fixing screws and carefully lift the board out, taking care not to damage the two indicators which protrude through the front panel. Finally slacken the screws in the terminal block behind the mains transformer and disconnect the mains wiring, again taking careful note of the positions of the wires.

Replacement is the reverse of the above. Make sure that the mains wiring is secured by the clip provided.

10.5.3 M24Fx

10.5.3.1 Preliminary

i) Before removing any part of the unit all cables should be disconnected and the plastic lid fitted. If the Panel board

is to be taken out, the fader and rotary control knobs must be removed before fitting the lid.

Each rotary control knob has a coloured plastic cover which should be carefully levered off to expose the securing collet. Unscrewing this, using a suitable tool, releases the knob. The fader knobs are a push fit and may be levered off, taking care not to damage the surface of the panel.

ii) Turn the console over so that the bottom is facing upwards and the rear extrusion towards you.

iii) Using a 'Posidrive' No 1 screwdriver, remove the eight screws around the extreme edge of the bottom cover. Note that two of the screws pass through the rubber feet; except on very early equipment, these will be those at back (wider end) of the unit. Raise the cover to obtain access to the power supply wiring.

The power supply chassis forms part of the cover and is connected to the rest of the unit by two cable assemblies, mains and low voltage. The low voltage cable assembly and the earth bond (the separate green/yellow wire) should be unplugged from the power supply unit. When removing the earth bond, do not pull the wire; the connector is of a special type which can only be removed by pulling the plastic shroud.

The cover may then be lifted to one side, taking care not to damage the mains wiring. If, however, there is insufficient working space available, the mains wiring may be disconnected at the screw terminal block on the power supply unit. Note the position of the wiring to ensure correct replacement.

Refitting is the reverse of the above. Ensure that all wiring and connectors are replaced correctly and that the cables are not trapped when the cover is replaced.

10.5.3.2 Power Supply Unit

The Power Supply unit forms part of the bottom cover of the console. Complete replacement cover assemblies are available from Rank Strand.

10.5.3.3 Panel Board

i) Remove the bottom cover of the console as described above.

ii) Disconnect the multiplex connectors from the Panel board, noting their positions to ensure correct replacement.

iii) Remove the eight screws fitted with grip washers which hold the Panel board in place. The eighteen screws securing the panel faders (those with plastic washers or, on some equipment, no washers at all) should not be removed. Lift the Panel board out of the console.

Replacement is the reverse of the above. The following should be noted, however:

i) The four-pin multiplex socket from the Multiplex Output connector on the rear of the unit normally connects to the centre of the three plugs on the Panel board (the other four-pin connector is only used on equipment using the four wire multiplex system).

ii) Lay the cables so that they will not be damaged when the bottom cover is replaced.

10.6 TEST PROGRAMS

To assist in diagnosing faults, M24 has a number of test facilities, some of which operate automatically each time the system is switched on. These tests are comprehensive and cover most parts of the system. It should be remembered, however, that the tests can only indicate where to start and are no substitute for normal service procedures.

1Ø.6.1 Power-up Self Tests

When the equipment is connected to the mains supply, four test procedures are carried out and the results are shown in the desk display windows and on the Video Mimic (if provided). If no fault is found, the desk windows will momentarily display dashes and then clear, and the top line of the Video Mimic will appear as follows:

M24 VERSION ** OUTPUT SELF TEST OK

The version number and 'SELF TEST OK' messages will disappear after about 8 seconds, leaving only the display heading. In addition to this, the 'MUX OK' indicators on the Multiplex Interface units should light. If any of these do not occur refer to Table 5.2.1 in the Operator's Handbook, which lists potential fault conditions and checks which should be carried out by the user. The checks listed only cover the most easily rectifiable faults and are intended to eliminate the obvious.

1Ø.6.2 Panel Tests

The operator-initiated tests are of two types, covering the Panel board and the Motherboard. In both cases, test mode is selected by operating the NMI button on the Panel board. The latter is located above the FADE button and, when the board is in situ, is accessible through a small hole in the panel; use a matchstick or a grub screwdriver to operate the button. Panel Test 1 is selected automatically on entering test mode.

The various tests are selected from the keypad and start immediately the number is entered. The current test may be stopped by pressing CL (Clear) or, if the next test in numerical order is required, by pressing '+1'.

Note: In the case of test 2 it is necessary to press the CL key twice to stop the test, because the first operation tests the button contact. This is also true of the '+1' button.

10.6.2.1 Test 1 - Display Test

When test 1 is selected, all of the displays and mimics flash at about once per second, in order that any which are inoperative may easily be seen. Note that, except for one on the keypad display, the decimal points in the windows are not used and will not light.

10.6.2.2 Test 2 - Contact Test

Selecting test 2 clears all of the displays. If any of the panel buttons are now operated, a corresponding code (see Table 10.6.2.1) will appear in the keypad and ACTIVE MEMORY windows.

Notes: 1) The codes for the REC LOCK keyswitch and the blackout switch will remain in the windows until the switch is returned to the off position or until another contact is operated. All other codes appear only while the appropriate button is held down.

2) The CL and '+1' buttons may each only be tested once. A second operation of CL terminates the test, while a second operation of '+1' selects test 3.

3) If the wheel is operated, the LEVEL window will count up or down as appropriate. The count will remain displayed while contacts are tested, but will be cleared by CL or '+1'. Note that the count will change much more rapidly than when the system is in normal operational mode, a count from 01 to 99 corresponding to a wheel movement of about a third of the exposed section.

10.6.2.3 Test 3 - Communication Test

This tests the serial link between the Panel board and the Motherboard in the control desk. When it is selected, the Panel processor counts the sync bytes received from the Motherboard and this is displayed in the keypad and ACTIVE MEMORY windows. The count should

increase in value about once per second; if this is not the case, a Motherboard fault is most likely.

10.6.2.4 Test 4 - Program Test

When this test is selected, the Panel PROM checksum is checked continually and the result displayed. If the checksum is correct, 00 appears in the keypad and ACTIVE MEMORY windows, while an error is indicated by a random pattern on the displays and indicators. Because the test is carried out continually, intermittent faults will cause a changing pattern to appear.

10.6.2.5 Test 5 - Select System Tests

Panel test 5 selects 'System Test' mode for testing the desk Motherboard.

Table 10.6.2.1

Panel Contact Numbers

Contact Number	Contact	Contact Number	Contact
00	0	17	CUE
01	1	18	CHANNEL
02	2	19	^ (Shift)
03	3	20	LINK
04	4	21	THRU
05	5	22	@
06	6	23	RETURN
07	7	24	FADE
08	8	25	SEQUENCE
09	9	26	MANUAL
10	+	27	USE TIME
11	-	28	BLACKOUT
12	.	29	RECORD BLIND
13	F	30	RECORD TOTAL
14	CLEAR	31	RECORD ENABLE
15	+1	32	FLASH OUT
16	MEMORY	33	FLASH FULL

10.6.3 System Tests

WARNINGS: 1) System Test 6 (Cue Store) will destroy the contents of the memories. Save important lighting cues on tape before starting this test.

2) System Test 7 (Analog Interface) will cause the luminaires controlled by the system to flash.

System Test mode is selected by entering Panel Test mode as described in section 10.6.2 above and then selecting test 5. On selection, the Video Mimic (sometimes referred to as the VDU) shows the following:

M24 SYSTEM TESTS

1 - VDU TEST (A)
2 - VDU TEST (B)
3 - MASTER & TIME FADERS
4 - TAPE INTERFACE
5 - PROGRAM CHECKSUM
6 - CUE STORE (CLEARS MEMORY!)
7 - ANALOG INTERFACE (FLASHES LIGHTS!)

TO RESUME NORMAL OPERATION, TURN SYSTEM OFF
AND ON AGAIN

ENTER TEST NUMBER FOLLOWED BY +1

This shows the tests available. If there is no Video Mimic, the tests may still be selected, but reference will have to be made to this handbook for the list.

The tests are selected by entering the required number on the keypad, followed by '+1' to start the selected test. If a number higher than 7 is selected when '+1' is pressed, the error number '199' will appear in the ACTIVE MEMORY window and the Video Mimic will display the message 'ILLEGAL TEST NUMBER - PRESS CLEAR'.

Once a test is running it may be stopped by pressing CL (Clear). Note that some tests will continue until the end of the current pass, which may take 2 to 3 seconds.

Certain tests may produce error messages on the Video Mimic. These are all presented in the same format; five headings with a series of numbers under each, as follows:

ERROR SUBTEST ADDRESS GOOD DATA BAD DATA

The precise meanings of the numbers associated with each error are described below in the individual test descriptions. When interpreting the results of a test, the terms 'GOOD DATA' and 'BAD DATA' should not be taken too literally.

10.6.3.1 VDU Test (A)

Sub-test 1

This test writes 25 lines of 64 characters (the complete character set) to the Video Mimic screen. Each line appears as follows.

@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_ !"#$%&'()*+,-./0123456789:;<=>?

Each line has a different attribute, starting with normal and followed by 'flashing', 'inverse', and 'dim', this sequence repeating every four lines.

Sub-test 2

If, having run sub-test 1, the '+1' key is operated, each character in the set will be written, in turn, to the whole screen, starting in the top left-hand corner. Each complete pass has a different attribute, in the same order as above. This test takes several minutes to complete.

10.6.3.2 VDU Test (B)

Sub-test 1

This test is similar to VDU Test (A), sub-test 1, but the characters are written one at a time, starting in the bottom right-hand corner.

Sub-test 2

As VDU Test (A) - sub-test 1, but when the screen is full the test repeats, starting with the next character in the set and the next attribute.

Video faults will show-up as anomalies in the otherwise regular patterns appearing on the display.

If no Video Mimic is provided, the above tests may still be selected and run, although they are of no practical use. The number of the selected test is shown in the keypad window and this may be cleared - stopping the test if it is in progress - by pressing the CL key.

10.6.3.3 Master and Time Faders

When this test is selected, the Video Mimic produces the following display:

M24 SYSTEM TESTS

3 - MASTER & TIME FADERS

75 F 00 22

The numbers shown represent the current settings of the four desk faders; i.e., from left to right, the MANUAL master fader, MEMORY master fader, the up fade-duration control (↑) and the down fade-duration control (↓). As the faders are moved from zero to full and vice versa, the numbers should change smoothly, without any jumps or hesitations.

The settings of the faders are also displayed in the LEVEL window on the desk, so that the test may be carried out on systems which do not have a Video Mimic. When the test is first selected, the level of the MANUAL master fader is displayed. Pressing '+1' will then select the MEMORY master fader and subsequent operations select the '↑' and '↓' controls, followed by a repeat of the sequence.

1Ø.6.3.4 Tape Interface

The Video Mimic produces the following display when this test is selected:

M24 SYSTEM TESTS

4 - TAPE INTERFACE PASS Ø1

Every time the Tape Interface tests are completed they restart from the beginning and the 'pass' number is incremented (the 'pass' number also appears in the LEVEL window on the desk). If a fault is found, an error message (see Table 1Ø.6.3.1) will be displayed on the Video Mimic and an error code in the ACTIVE MEMORY window on the desk. Should the same fault(s) be found on each pass (as is most likely) the test will continue until the Video screen is full, when it will stop, this condition being indicated by the 'Tape' indicator on the desk flashing. The screen may then be cleared and the test resumed by pressing '+1'.

1Ø.6.3.5 Program Checksum

This is a test for program errors. It operates in a similar way to test 4. The checksum is calculated separately for each PROM and compared with the correct value stored in the 'Kernel' PROM.

1Ø.6.3.6 Cue Store

WARNING: The Cue Store test destroys the contents of the memories. Save important lighting cues on tape before selecting this test.

This test is similar to the previous two, but can only be carried out if the REC LOCK keyswitch is in the horizontal, enabled position. Only the Cue memory is tested (addresses $1ØØØ to $3FFF on standard systems), the various working stores, etc. being checked on power-up. If, however, bit 5 of system configuration switch SW1 is set, the test assumes that expansion memory is fitted, and will

attempt to test up to $7FFF, producing error messages for the non-existent RAM.

If the memory test is terminated normally (by pressing CLEAR while the test is running), it will automatically clear the Cue memory before returning to test selection mode.

10.6.3.7 Analogue Interface

WARNING: This test will cause the luminaires controlled by the system to flash. To prevent this, remove the MULTIPLEX O/P connector at the rear of the desk or switch off the power to the dimmers before selecting the test.

This tests the circuits which transmit to and receive from the Multiplex Interface unit(s), and also the panel fader analogue-to-digital converter. The test is similar to the previous three.

10.6.4 Returning to Normal Operation

On completion of the operator-initiated tests, the system should be returned to normal operation by momentarily switching off the mains supply.

Table 10.6.3.1

ERROR NUMBERS

Error	Meaning	Notes
41	Tape ACIA Tx timeout (failed to go ready)	ADDRESS = $8006 (ACIA status register) GOOD DATA = 00 BAD DATA = ACIA status
42	Tape ACIA Rx timeout	ADDRESS = $8006 (ACIA status register) GOOD DATA = 00 BAD DATA = ACIA status
43	Tape ACIA Status Error	ADDRESS = $8006 (ACIA status register) GOOD DATA = 00 BAD DATA = ACIA status
44	Tape ACIA Data Error	ADDRESS = $8007 (ACIA data register) GOOD DATA = Data transmitted BAD DATA = Data received
51	Kernel PROM checksum error	ADDRESS = $E000 (base address of PROM) GOOD DATA = checksum expected BAD DATA = actual checksum
52	Page 0 PROM checksum error	ADDRESS = $A000 (base address of PROM) GOOD DATA = checksum expected BAD DATA = actual checksum
53	Page 0 PROM checksum error	ADDRESS = $C000 (base address of PROM) GOOD DATA = checksum expected BAD DATA = actual checksum
60	Cue memory test - REC LOCK keyswitch in 'locked' position	-

Table 10.6.3.1 (cont.)

ERROR NUMBERS

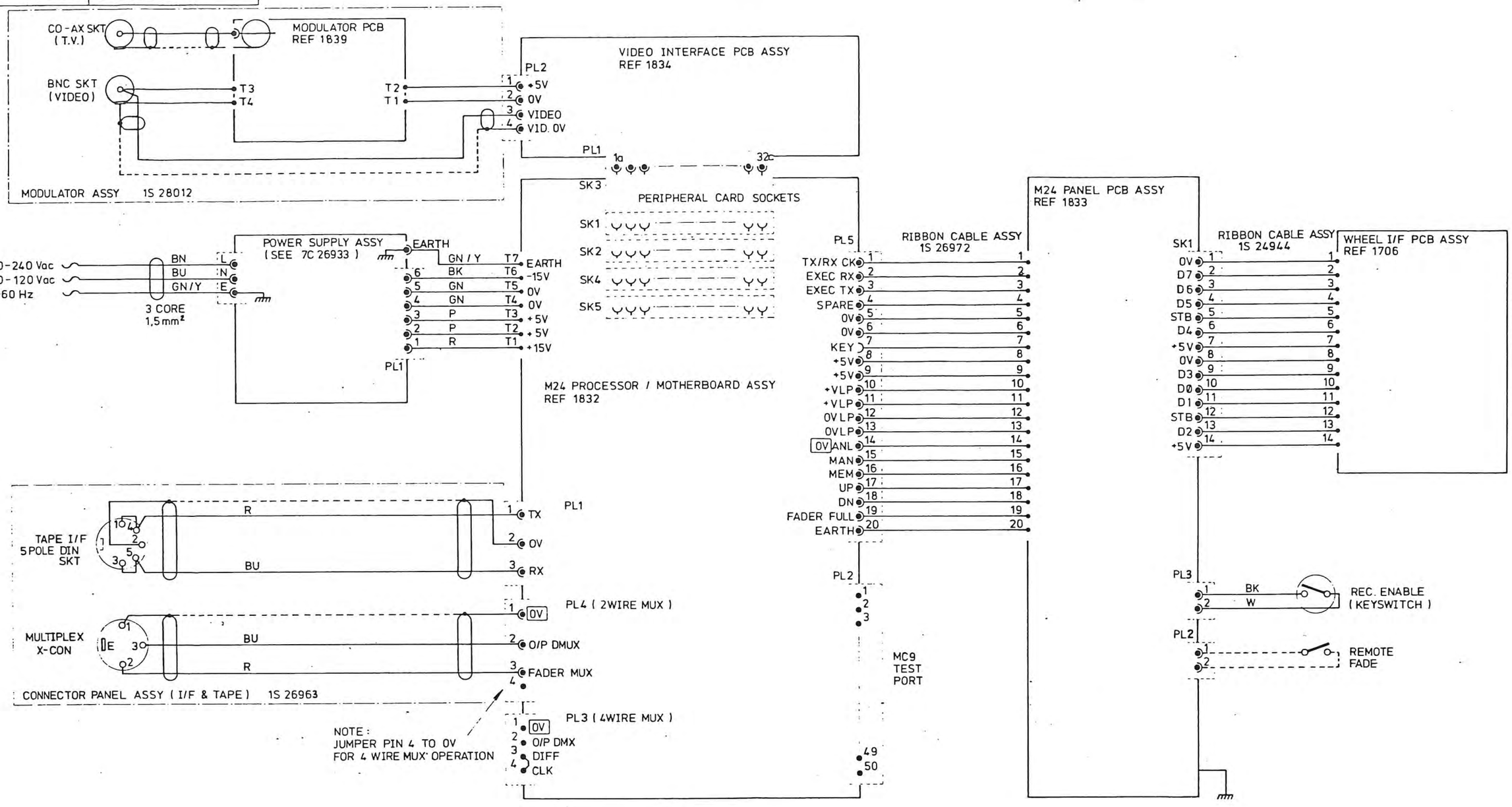
Error	Meaning	Notes
61	Memory test failed on simple write/verify of entire memory	ADDRESS = failing location GOOD DATA = data written to memory BAD DATA = data read back from memory
62	Memory failed on writing low order address byte of location into that location.	ADDRESS = failing location GOOD DATA = data written to memory BAD DATA = data read back from memory
63	Address line failure	ADDRESS = failing location GOOD DATA = data written to memory BAD DATA = data read back from memory
64	Data line failure.	ADDRESS = failing location GOOD DATA = data written to memory BAD DATA = data read back from memory
65	Pattern written to memory failed to verify	ADDRESS = failing location GOOD DATA = data written to memory BAD DATA = data read back from memory
66	Immediate write/verify of two consecutive locations failed.	ADDRESS = failing location GOOD DATA = data written to memory BAD DATA = data read back from memory
70	Analog 0V on input 6 of multiplexer too high	ADDRESS = $800A (A/D converter) GOOD DATA = 00 BAD DATA = data read from A/D converter
71	Mux output low when $FF written to D/A converter	ADDRESS = $800A GOOD DATA = $FF BAD DATA = data read from A/D converter Note: Although the good data is shown as $FF, the test will accept down to $C0 to allow for the range of adjustment on the Mux output.

Table 1Ø.6.3.1 (cont.)

ERROR NUMBERS

Error	Meaning	Notes
72	Mux output out of range when $ØØ written to D/A converter	ADDRESS = $8ØØA (A/D converter) GOOD DATA = $ØØ BAD DATA = data read from A/D converter Note: Although the good data is shown as $ØØ, the nominal value read back from the A/D converter will be about $8Ø, because of the potential divider feeding input 7 of the multiplexer. The test allows for this and also +/-$2Ø on this value to allow for tolerances.
73	Analog ramp failure. A 15 step ramp from $1Ø to $FØ is output and checked. One of the levels came back as less than the previous level.	ADDRESS = $8ØØA (A/D converter) GOOD DATA = data written to D/A converter BAD DATA = data read from A/D converter Note: The BAD DATA value will be affected as noted above.
74	Sync level too high	ADDRESS = $8ØØA (A/D converter) GOOD DATA = ØØ BAD DATA = data read from A/D converter

DWG. No. 7B26998 | ISSUE ~~A~~ ~~B~~ C



REV.1 C.No.E5035 DIN SKT. RENUMBERED RDK 18.3.83

REV.2 E5044 PL2 & PL3 ON REF 1833 REVERSED

Rank Strand Ltd.

PO Box 51 Great West Road Brentford Middlesex TW8 9HR Telephone 01-568 9222 Telex 27976

DIMENSIONS IN INCHES/MILLIMETRES

THIRD ANGLE PROJECTION

TOLERANCES	
IMPERIAL	METRIC
FRACTION ± 1/64"	1 DEC PLACE ± 0.4mm
DECIMAL ± .005"	2 DEC PLACE ± 0.1mm
ANGULAR ± 0.25	
UNLESS OTHERWISE STATED	
USED ON:- 1L 26980	
M24	

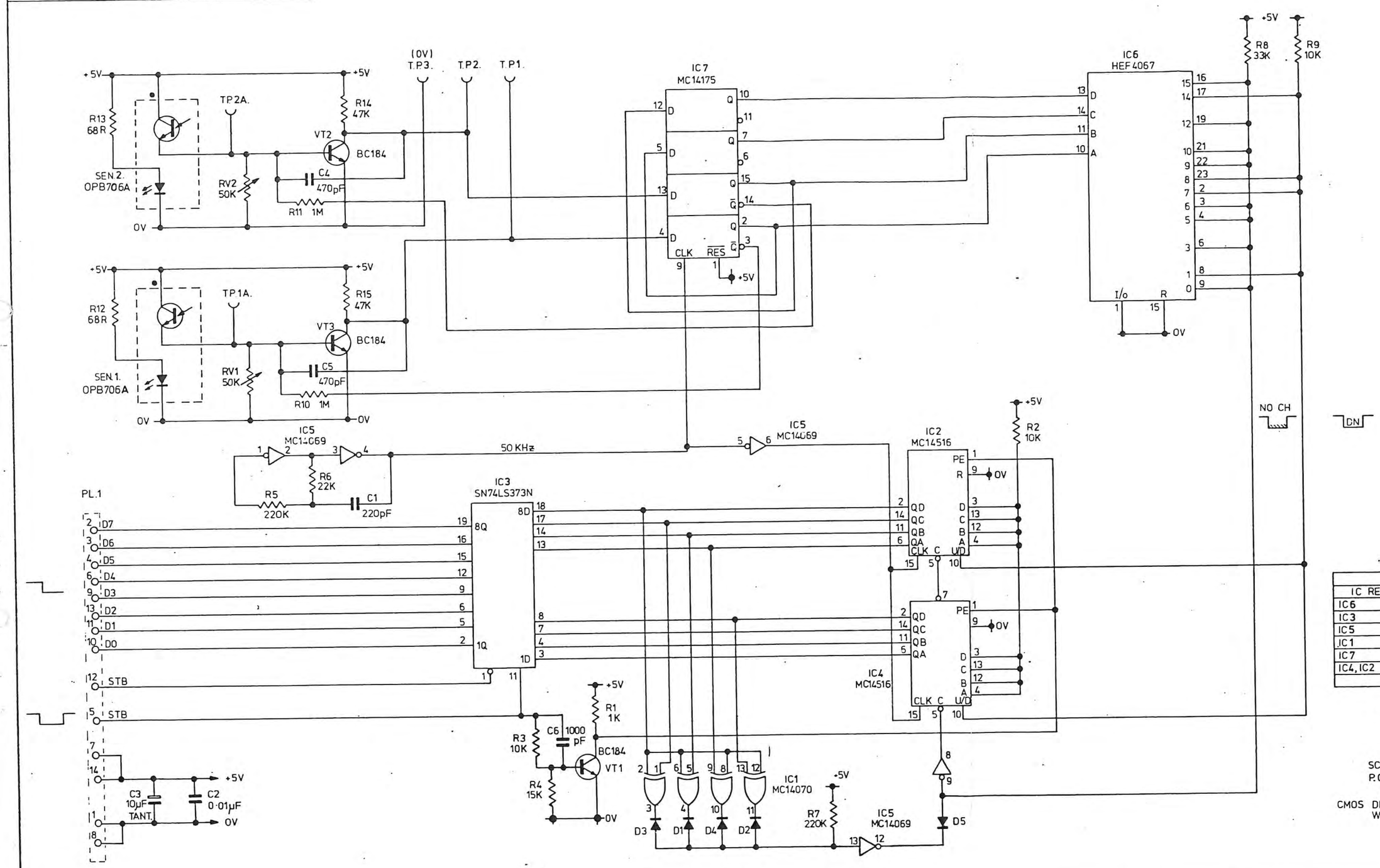
SCALE	—	DATE
DRAWN	RDKirsby	6.10.82
CHECKED	[signature]	11:11:82
APPROVED	[signature]	4/11/82
MATERIAL:-	—	
FINISH	—	

TITLE:- TEMPUS M24 DESK WIRING DIAGRAM

ISSUE ~~A~~ ~~B~~ C

DWG. No.7B 26998

DWG. Nº 6B24310 | ISSUE 123



INTEGRATED CIRCUITS			
IC REF	TYPE	Vcc	0V
IC6	HEF 4067BP	24	12
IC3	SN74LS373N	20	10
IC5	MC14069BCP	14	7
IC1	MC14070BCP	14	7
IC7	MC14175BCP	16	8
IC4, IC2	MC14516BCP	16	8

ALL DIODES IN914

SCHEDULE 5S24311
P.C. BOARD 5B24312

CMOS DEVICES USED, AVOID STATIC WHEN HANDLING.

REV.1 C.Nº
RAISED TO PROD. ISS.
CHANGED 30.1.81
APPROVED 26-2-81
REV.2 C.N. E4468
SENSORS 1 & 2 WERE FPA 103 S.
D.E. Naish 9.12.82
REV.3 E5071
SENSORS 1 & 2 WERE FPA 105
20/6/83

RANK STRAND ELECTRIC
PO BOX 70 Great West Road Brentford Middlesex TW8 9HR
Telephone 01-568 9222 Telex 27978
A DIVISION OF
RANK AUDIO VISUAL LIMITED

DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

TOLERANCES			
IMPERIAL	METRIC		
FRACTION ± 1/64"	1 DEC PLACE ± 0·4mm		
DECIMAL ± ·005"	2 DEC PLACE ± 0·1mm		
ANGULAR ± 0·25°			
UNLESS OTHERWISE STATED			
USED ON:- 1L24344			

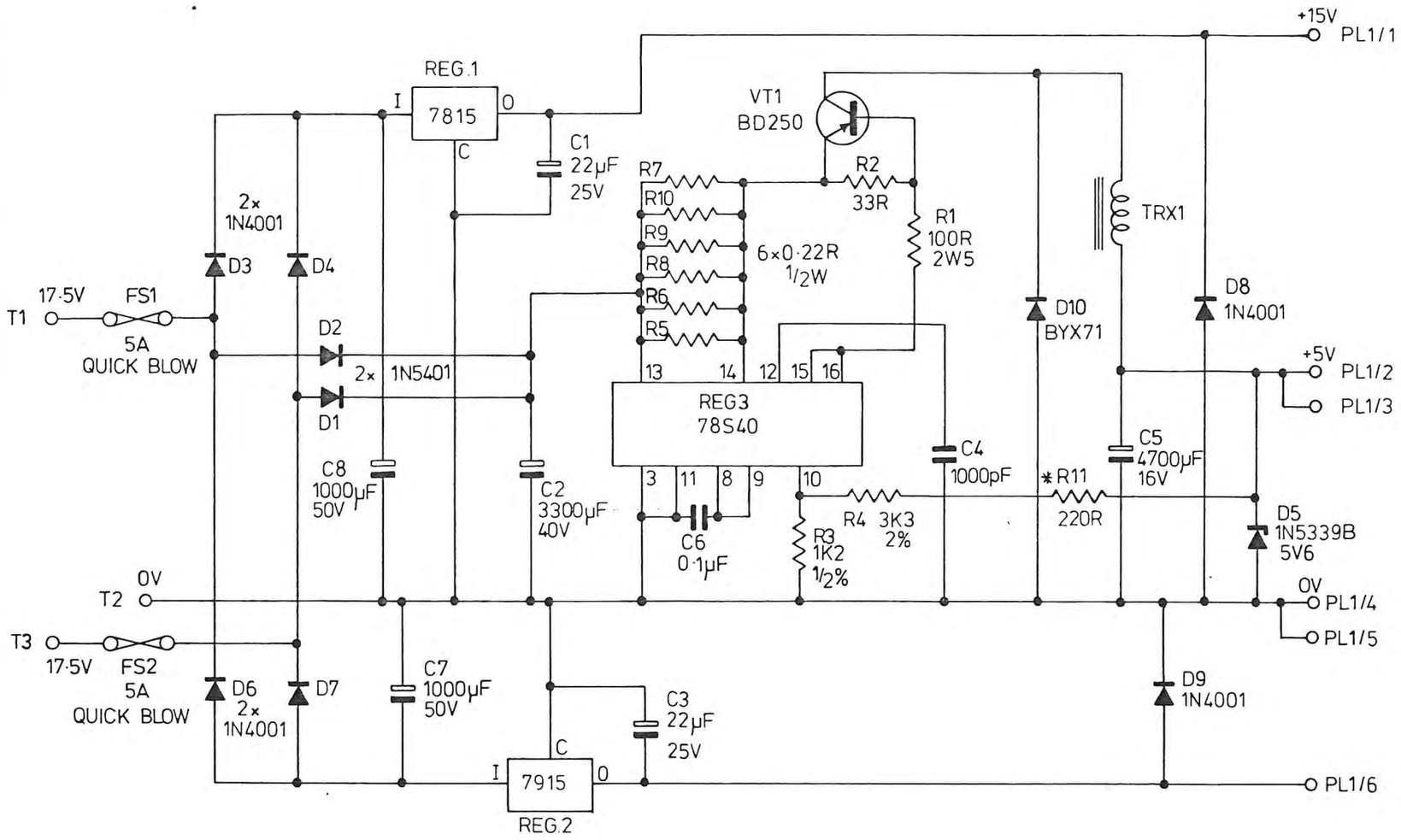
SCALE		DATE
DRAWN	D.E. NAISH	4·9·79
CHECKED		26-2-81
APPROVED		
MATERIAL:-		
FINISH:-		

TITLE:-
DDM3 WHEEL INTERFACE CIRCUIT DIAGRAM.

P.C.B. 764/3 REF. 170

ISSUE 123 DWG. Nº 6B24310

DWG. Nº 6C26865 | ISSUE ~~A~~ ~~B~~ ~~C~~ D



*NOTE RESELECT ON TEST IF O/P VOLTAGE IS OUTSIDE 4·9V–5·1V RATIO IS 1mV = 1Ω

P.C.BOARD - 5B26866.
SCHEDULE - 5S26867.

REV.1. C.Nº ES003
RI ACCESS. CIRCUIT UPDATED TO NEW ISSUE 3 P.C.B.
D.E.Naish 22.8.83
24-2-83

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PO Box 51 Great West Road Brentford Middlesex TW8 9HR
Telephone 01-568 9222 Telex 27976
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DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

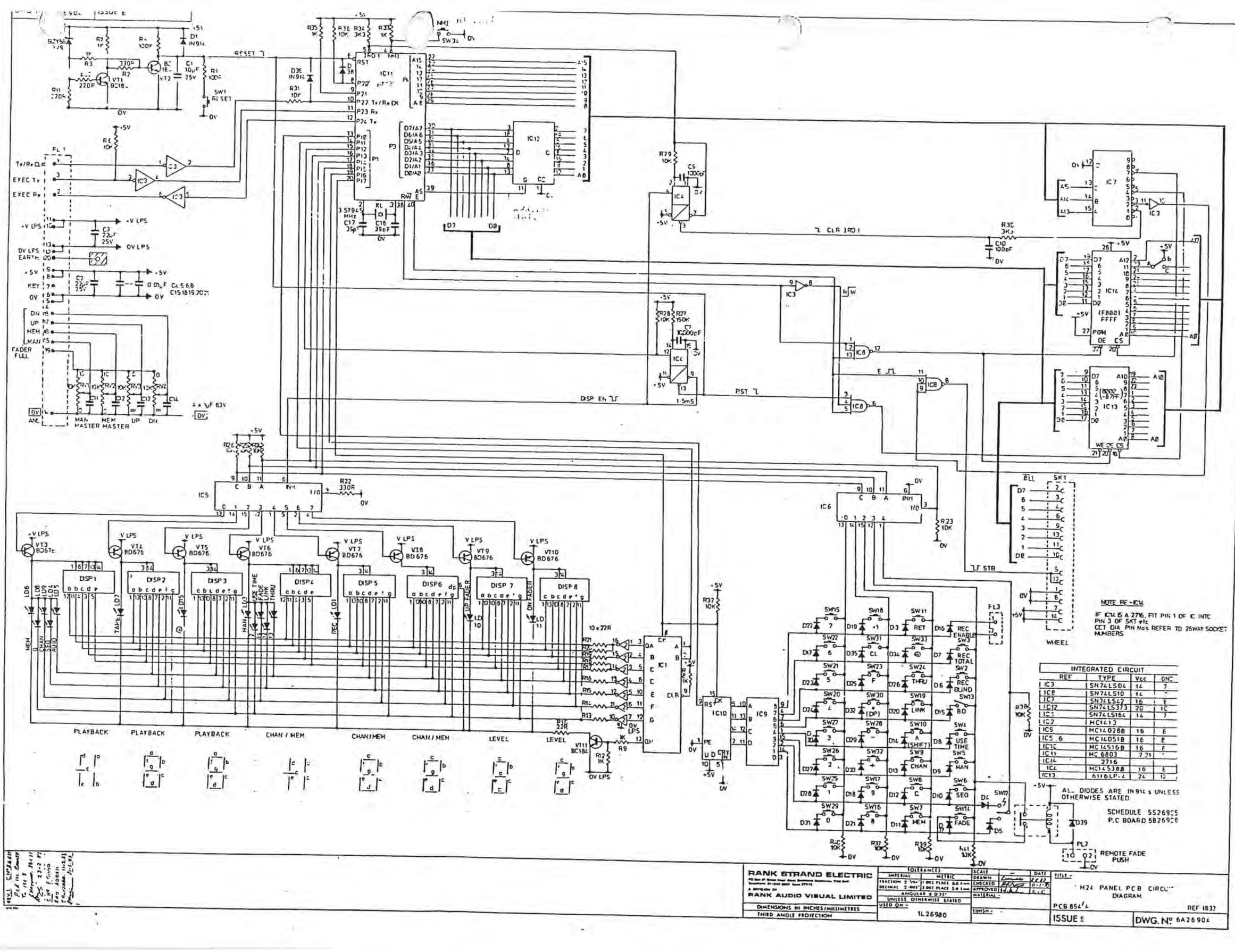
TOLERANCES	
IMPERIAL	METRIC
FRACTION ± 1/64"	1 DEC PLACE ± 0·4 mm
DECIMAL ± ·005"	2 DEC PLACE ± 0·1 mm
ANGULAR ± 0·25°	
UNLESS OTHERWISE STATED	
USED ON :-	1L26980
M24 DESK PSU	

SCALE	N.T.S	DATE
DRAWN	D.E.NAISH	6·7·82
CHECKED	[signature]	11:1:83
APPROVED	[signature]	11:1:83
MATERIAL :-		
FINISH :-		

TITLE :-
M24 POWER SUPPLY BOARD.
PCB 850/3 REF. 1830

ISSUE ~~A~~ ~~B~~ ~~C~~ D | DWG. Nº 6C26865

WW 289



INTEGRATED CIRCUIT			
REF	TYPE	Vcc	GND
IC3	SN74LS04	14	7
IC8	SN74LS10	14	-
IC7	SN74LS42	16	8
IC12	SN74LS373	20	10
IC?	SN74LS164	14	7
IC2	MC1413		
IC9	MC14028B	16	8
IC5 6	MC14051B	16	8
IC10	MC14516B	16	8
IC11	MC 6803	7.21	-
IC14	2716		
IC4	MC14538B	16	8
IC13	6116LP-2	24	12

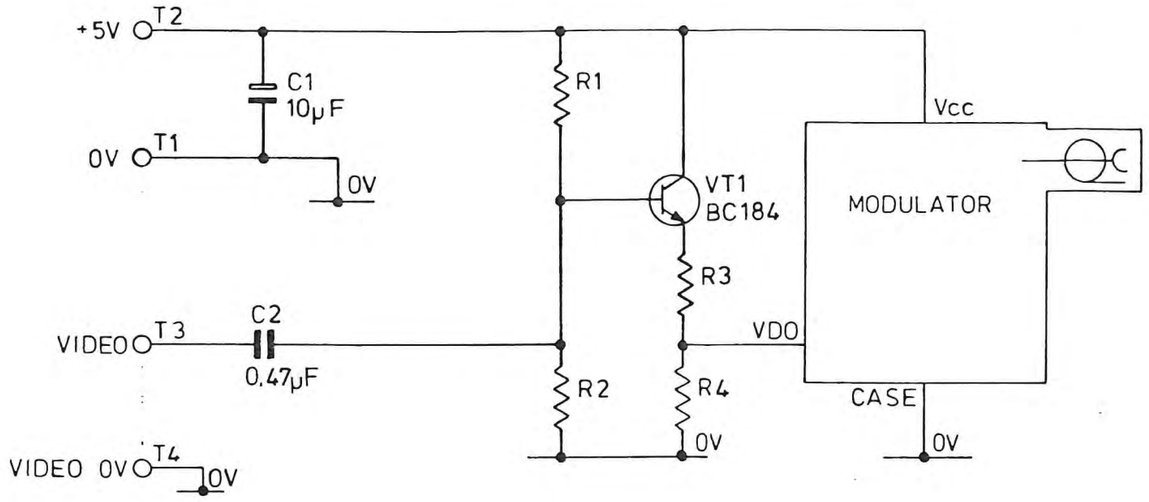
RANK STRAND ELECTRIC
A division of RANK AUDIO VISUAL LIMITED
DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

TOLERANCES: IMPERIAL / METRIC
FRACTION ± 1/64" — 1 DEC PLACE ± 0.5 mm
DECIMAL ± .005" — 2 DEC PLACE ± 0.1 mm
ANGULAR ± 0.25°
UNLESS OTHERWISE STATED
USED ON - 1L26980

SCALE - | DRAWN | CHECKED | APPROVED | MATERIAL - | FINISH -
DATE

TITLE - M24 PANEL PCB CIRCUIT DIAGRAM
PCB 85[illegible]
REF 1832
ISSUE E
DWG. Nº 6A26904

DWG. Nº 6C 28009	ISSUE A B C



COMP. REF	COMP. VALUE / TYPE	
	REF 1839 / A (VHF)	REF 1839 / C (UHF)
R1	82K	15K
R2	39K	120K
R3	22 SWG T.C.W.	680R
R4	100R	1K8
MODULATOR	1082	1233

COMPONENT VARIATIONS.

	MODULATOR TYPE	
	1082	1233
VDO	1	2
Vcc	2	3
0V	CASE	CASE

MODULATOR LEAD ASSIGNMENTS.

SCHEDULE – 5S 28010

P.C.BOARD – 5C 28011

REV.1. C.Nº E6002
REF 1839/A - A1+R2 WERE 33K. R3 WAS 150 Ω.
17/6/83

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PO Box 51 Great West Road Brentford Middlesex TW8 9HR
Telephone 01-568 9222 Telex 27976
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DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

TOLERANCES	
IMPERIAL	METRIC
FRACTION ± 1/64"	1 DEC PLACE ± 0·4 mm
DECIMAL ± ·005"	2 DEC PLACE ± 0·1 mm
ANGULAR ± 0·25°	
UNLESS OTHERWISE STATED	
USED ON :- 1L 26980	
M24	

		DATE
SCALE	—	
DRAWN	PDKirkby	12.10.82
CHECKED	M.A. Arbe	21.1.83
APPROVED		21:1:83
MATERIAL :-	—	
FINISH :-	—	

TITLE :-
MODULATOR P.C.BOARD
CIRCUIT DIAGRAM
PCB 864/1
REF 1839 / A
REF 1839 / B

ISSUE A B C

DWG. Nº 6C 28009

WW 289

DWG. N° 6A 26940 | ISSUE -

ADDRESSES		
BASE ADDRESS Ø	NORMALLY 8015	NOT USED
" +1	" 8015	VDU CHARACTER
" +2	" 8016	REGISTER POINTER
" +3	" 8018	REGISTER DATA

INTEGRATED CIRCUITS			
IC REF	IC TYPE	0V	+5V
IC13	DM86S64 CABN	8	16
IC12	6116 - 3P	12	24
IC11	SY 6545A-1	1	20
IC 9	SN74LS74N	7	14
IC18	SN74LS161N	8	16
IC14,16	SN74LS75	12	5
IC15	SN74LS11		
IC3	SN74LS00	7	14
IC1	SN74LS27	7	14
IC17	SN7404	7	14
IC8	SN74LS240	10	20
IC7	SN74LS04	7	14
IC4	SN74LS38	7	14
IC5,6	SN74LS136	7	14
IC2	SN74LS123	8	16
IC10	MC14024BCP	7	14

ALL DIODES ARE IN914's UNLESS OTHERWISE STATED

SCHEDULE _ 5S26941

PCB DRILLING _ 5B 26942

REV.1 C.N°

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DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

TOLERANCES
IMPERIAL | METRIC
FRACTION ± 1/64" | 1 DEC PLACE ± 0·4mm
DECIMAL ± .005" | 2 DEC PLACE ± 0·1mm
ANGULAR ± 0·25°
UNLESS OTHERWISE STATED
USED ON :- 1L26980
M24

SCALE —
DRAWN P.D.Kemp 26.8.82
CHECKED P.J.Barker 30.8.82
APPROVED [illegible] 31.8.82
MATERIAL - —
FINISH :- —

TITLE :- M24 VIDEO INTERFACE CIRCUIT DIAGRAM
PCB 855/2 REF 1834
ISSUE C | DWG. N° 6A 26940

DWG. Nº 6A26932 SHT 1 OF 2 SHTS | ISSUE A B C D E

T1 +15V
T2 +5V
T3
T4 0V
T5
T6 -15V
T7 GND

C26 22µF 25V
C27 1000µF 10V
C28 22µF 25V
C15,7, 8,13-16, 19,21, 24,25, 29,30, 32-35, 38,43, 44 — 21×0·01µF

+15V R32 10K 2% VT1 BC184 D15 BZY88 3V3 R36 1K SW3 RESET
+5V R34 1K R35 10K R39 10K VT3 BC184 VT2 BC184 VT4 BC184 VT5 BC184 R37 10K R38 10K D17
C23 22µF 25V
R31 6K8 2% R33 100
0V

4·9152MHz
153·6KHz
MRDY
IRQ
8000 - BDFF
VPA (BDFE - BFFF) Valid peripheral address
RESET
D0 - D7
A0 - A15
XX00 - XX0F

IC11 R21 1K R22 1K
A15 IC15 IC16
VPA IC14
CSO for IC21/22/23 OE1

MC9 TEST PORT
LD7 6 5 4 3 2 1 LDX LDATA LMC LIRQ LFIRQ LRST LBREQ HALT LE LD SYNC
PL21 RN2 1K
LBS LBAL R/W LA LVMA +5V 0V KS
R41 22K R35 1K 33·35 37·39 41·43 45

IC23 6809
C22 1µF TANT 16V
D0 D7 A0 A15 R/W E Q BA BS
NMI IRQ FIRQ DMA/BREQ RES HALT MRDY
XTAL EXTAL X1·2 8MHz C17 15pF C18 18pF LK1

IC18 IC19 SKT 1-5
A0 A15 VMA D0 RESET MRDY FIRQ IRQ NMI 0V E R/W VPA 156·3KHz PR2 PR1 PR0 0V -15V +15V +5V 0V ANL FADER FULL ANL OUT

R2C 220R R15 3K3 RN1/2 RN1 1K IC2C

IC36 IC47 IC53 IC41 IC40 IC56 IC37 IC33 IC35 IC10 IC17

PR2 PR1 PR0
WRITE INH. RW E M LOCK
OE RAM 22
VT13 2N222 R63 330R
DIR IC17 (from Z80 buffer)
DIR=L DIR=H DIR EN

RESET
-VRAM
IC38 IC42 IC48 IC54 IC39 IC43 IC49 IC55
RN4 1K
IC32 IC34
R85 1K R50 1K

BATT VT11 2N3702 R84 220R R83 220R D2L 1N003 C47 22µF 25V C48 C45 C36 2×0·01µF +VRAM
IRQ IC11

IC22 E000 - FFFF
IC25 C000 - DFFF
IC29 A000 - BFFF
LK2

R86 R87 R88 3×10K R47 1K
PROM PROM CE6 PROM CE7 CE5 LK3 LK5 LK4
RN5 10K RN3 10K

PC BOARD - 5B26930
SCHEDULE - 5526931
BUS SIGNAL SPEC - 1C28030

REV.1 CAPACITORS ADDED ON CLOCK TO RAM LINES AND DATA BUS. R47 CHANGED FROM 330R. R9 and C21 OMITTED. Changed 16.4.81 Changed 19.5.81

RANK STRAND ELECTRIC
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A DIVISION OF RANK AUDIO VISUAL LIMITED
DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

TOLERANCES		SCALE	—	DATE
IMPERIAL	METRIC	DRAWN	DE NASH	6.5.80
FRACTION ± 1/64"	1 DEC PLACE ± 0·4 mm	CHECKED		11.5.81
DECIMAL ± ·005"	2 DEC PLACE ± 0·1 mm	APPROVED		4.6.81
ANGULAR ± 0·25°		MATERIAL	—	
UNLESS OTHERWISE STATED		FINISH	—	
USED ON - 1L26980				

TITLE - M24 MOTHERBOARD AND PROCESSOR CARD
PCB 853/5 REF 1832
ISSUE A B C D E | DWG. Nº 6A26932 | SHT 1 OF 2 SHTS

DWG. N° 6A26932 SHT 2 OF 2 SHTS | ISSUE A B C D E

INTEGRATED CIRCUITS

IC REF	TYPE	VCC	GND	IC REF	TYPE	VCC	GND
IC13	SN74S04N	14	7	IC37	MC1408L8-8	13	-
IC22	SN74S74N	14	7	IC38	MC1456P	-	-
IC41	SN74S51N	14	7	IC39	MC1013BCP	14	-
IC44	SN75154N	24	4	IC41	MC1013BCP	14	-
IC1,42	SN74LS00N	14	7	IC6	MC14027BCP	16	B
IC31	SN74LS32N	14	7	IC9	MC14040BCP	16	E
IC15,16,37	SN74LS04N	14	7	IC4	MC14066BCP	16	E
IC36	SN74LS20N	14	7	IC32	MC14021BCP	16	E
IC47	SN74LS38N	14	7	IC3	MC1455P8	8	-
IC35	SN74LS42N	16	8	IC5	MC1455P8	8	E
IC27	SN74LS85N	16	8	IC23	MC68B09E	7	1
IC12	SN74LS93N	14	10	IC21	MC68B21P	24	1
IC24	SN74LS139N	16	8	IC24,28	MC68B50P	12	1
IC11	SN74LS136N	14	7	IC45	TL084 ACN	-	-
IC2,43	SN74LS156N	16	8	IC26	AD7574JN	1	1E
IC10,18,19	SN74LS240N	20	10	IC46	LM311P	-	-
IC30,32	SN74LS241N	20	10	IC22,25,29	2764-4	28	1
IC17	SN74LS374N	20	10	IC33,34,42,43,46	HM6116LP-4	24	1
IC33,1E	SN74LS640N	20	10	4N54,55			

NOTE ALL DIODES 1N914 UNLESS OTHERWISE STATED

REVI	C.N. 31604
	Issued to Cust
	ICs with sockets
	Add Diode D19
	Add Diode D21
	Add Diode D22
	Add Diode D23
	Add Diode D24
	Add Diode D25
	Add Diode D26
	Add Diode D27
	Add Diode D28
	Add Diode D29
	Add Diode D30
	Add Diode D31
	Add Diode D32
	Add Diode D33
	Add Diode D34
	Add Diode D35
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	Add Diode D141
	Add Diode D142
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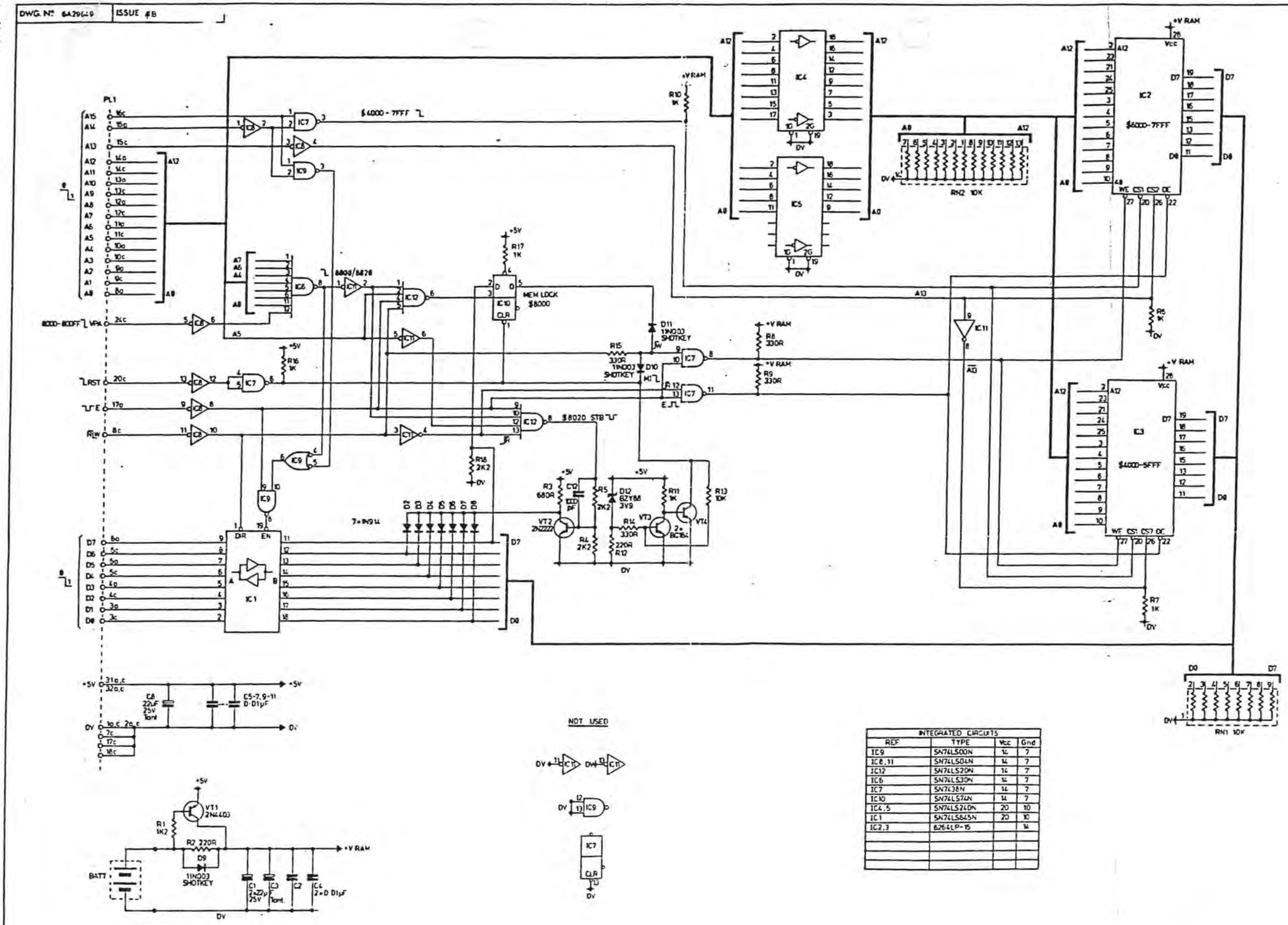
RANK STRAND ELECTRIC
A DIVISION OF RANK AUDIO VISUAL LIMITED

TOLERANCES: IMPERIAL / METRIC; FRACTION ± 1/64" | 1 DEC PLACE ± 0.4mm; DECIMAL ± .005" | 2 DEC PLACE ± 0.1mm; ANGULAR ± 0.25°; UNLESS OTHERWISE STATED
USED ON - 1L26980
DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

SCALE —
DRAWN DE NAISH 8-9-82
CHECKED
APPROVED
MATERIAL -
FINISH -

TITLE - M24 MOTHERBOARD AND PROCESSOR CARD
PCB853/3 REF 1832
ISSUE A B C D E
DWG. N° 6A26932 SHT 2 OF 2 SHTS

DWG. Nº 6A29649 | ISSUE #B



INTEGRATED CIRCUITS			
REF	TYPE	Vcc	Gnd
IC9	SN74LS00N	14	7
IC8,11	SN74LS04N	14	7
IC12	SN74LS20N	14	7
IC6	SN74LS30N	14	7
IC7	SN7438N	14	7
IC10	SN74LS74N	14	7
IC4,5	SN74LS240N	20	10
IC1	SN74LS645N	20	10
IC2,3	6264LP-15		14

SCHEDULE - 5S29650
P.C.BOARD - 5C29651

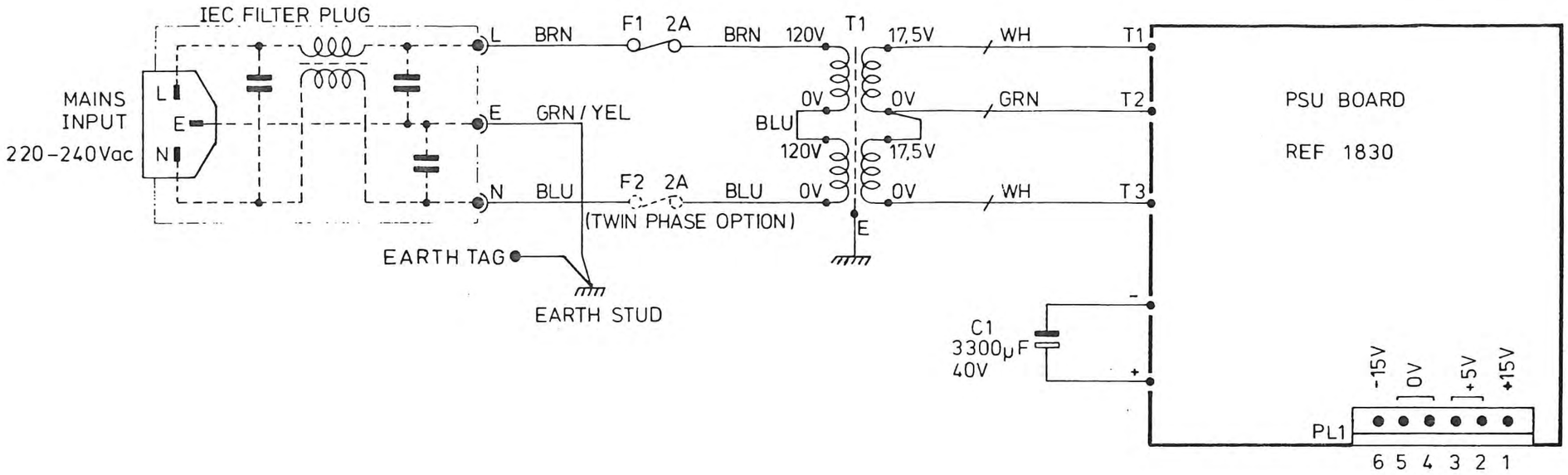
RANK STRAND ELECTRIC
RANK AUDIO VISUAL LIMITED
DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

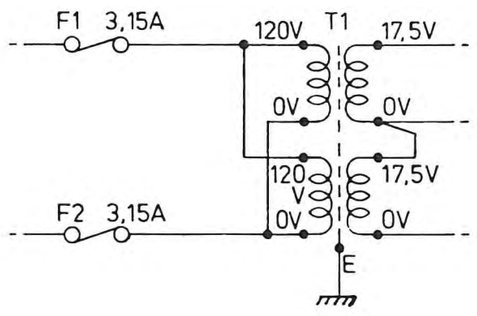
TOLERANCES: IMPERIAL / METRIC — ANGULAR ± 0.25° — UNLESS OTHERWISE STATED
USED ON: M24 1L26980

SCALE — DRAWN J.E. NAISH 15.2.85 — CHECKED — APPROVED — MATERIAL — FINISH

TITLE: M24 16K MEMORY EXPANSION CARD
PCB 914/1 — REF 1679
ISSUE #B — DWG. Nº 6A29649

DWG. Nº 7C 26933 | ISSUE ~~A~~B





110V OPTION

WIRE SIZES

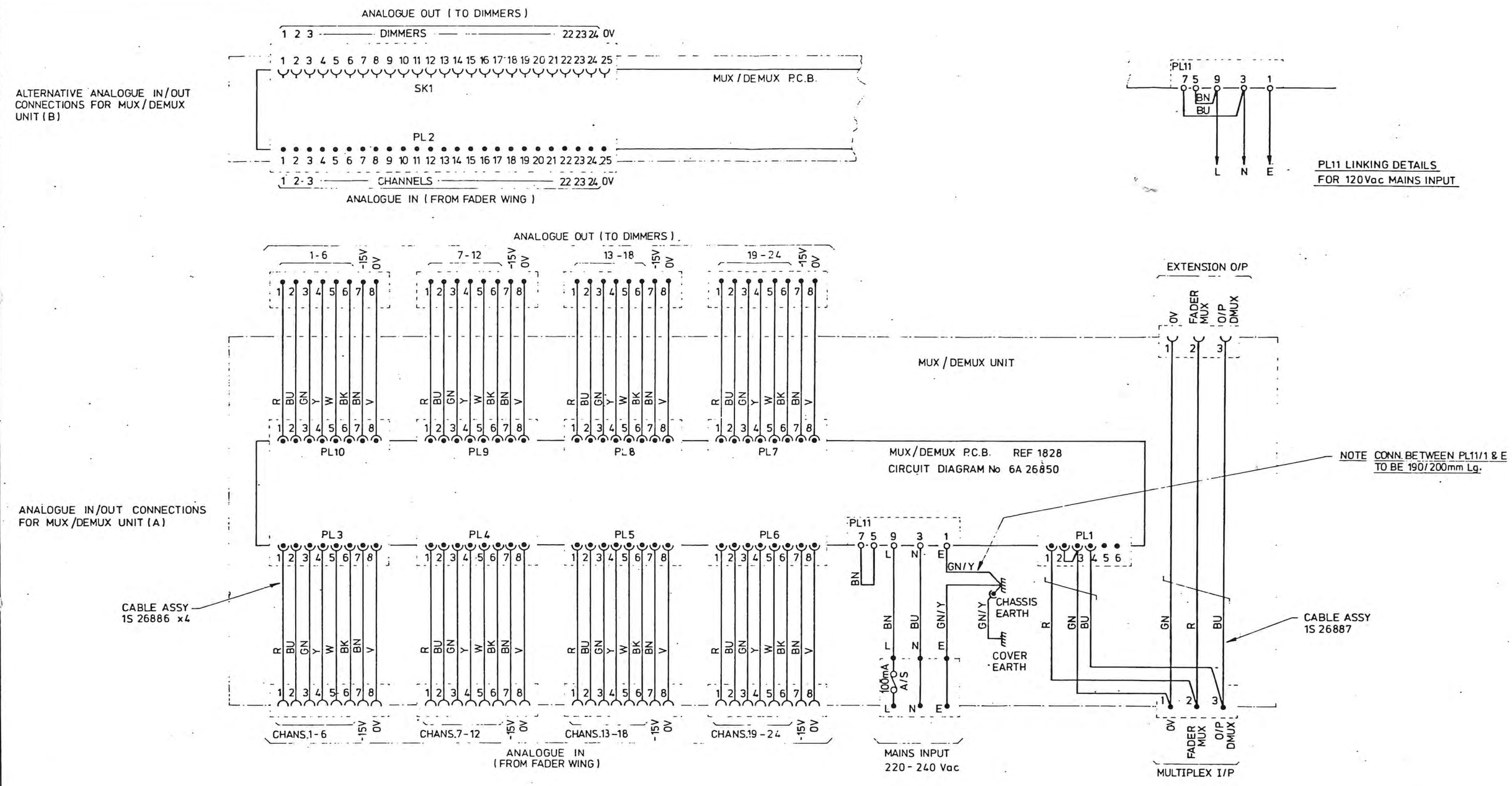
1,5 mm²

0,75 mm²

REV. 1. C. Nº E5077 TRX-'E' STUD LINK DELETED. 20/6/83 21-6-83	RANK STRAND ELECTRIC PO Box 51 Great West Road Brentford Middlesex TW8 9HR Telephone 01-568 9222 Telex 27976 A DIVISION OF RANK AUDIO VISUAL LIMITED	TOLERANCES IMPERIAL / METRIC FRACTION ± 1/64" / 1 DEC PLACE ± 0·4 mm DECIMAL ± ·005" / 2 DEC PLACE ± 0·1 mm ANGULAR ± 0·25° UNLESS OTHERWISE STATED	SCALE —— DATE DRAWN RD Kiral Cy 18.8.82 CHECKED [signature] 11:11:82 APPROVED D. Hertendorf 12.11.82	TITLE :- PSU WIRING DIAGRAM	
	DIMENSIONS IN ~~INCHES~~/MILLIMETRES THIRD ANGLE PROJECTION	USED ON :- 1L 26980 M24	MATERIAL :- FINISH :-	ISSUE ~~A~~B	DWG. Nº 7C 26933

WW 280

DWG. No. 7B 26872 | ISSUE ~~A~~ ~~B~~ C



SCHEDULES :—

MUX / DEMUX UNIT (A) 1S 26869

MUX / DEMUX UNIT (B) 1S 26871

REV.1 C.No.E5057 PL Nos REVISED PL11 LINK 7-5 ADDED. RDK 25.5.83	REV2 E5092 NOTE RE LENGTH OF 'E' CONN'N ADDED	Rank Strand Ltd. PO Box 51 Great West Road Brentford Middlesex TW8 9HR Telephone 01-568 9222 Telex 27976	TOLERANCES IMPERIAL / METRIC: FRACTION ± 1/64" 1 DEC PLACE ± 0.4mm; DECIMAL ± .005" 2 DEC PLACE ± 0.1mm; ANGULAR ± 0.25; UNLESS OTHERWISE STATED	SCALE —	DATE	TITLE:- MUX / DEMUX UNIT WIRING DIAGRAM.	
		DIMENSIONS IN INCHES/MILLIMETRES	USED ON:- IL 26980	DRAWN	13.10.82		
		THIRD ANGLE PROJECTION	M24	CHECKED			
				APPROVED	15-10-82		
				MATERIAL:- —			
				FINISH:- —		ISSUE ~~A~~ ~~B~~ C	DWG. No. 7B 26872

DWG. N° 6A26850 | ISSUE D

INPUT RANGE	R48 1/2%		R73 1/2%	
	+ ve	- ve	+ ve	- ve
15V	5K00	3K33	20K0	30KC
10V	10K0	5K00	10K0	20KC
5V	—	10K0	LINK	10K0

NOTE ALL DIODES ARE ISS2C UNLESS OTHERWISE STATED

FOUR WIRE MULTIPLEX

TWO WIRE MULTIPLEX

24 x 100K

24 x 10K FOR AN BN OPTION
24 x 1K FOR AP, BP OPTION

24 x 0·33μF

8 x 10K RN1

8 x 10K RN2

8x 10K RN3

* C5 FITTED AND C6 OMITTED FOR AP, BP OPTION
C6 FITTED AND C5 OMITTED FOR AN, BN OPTION

240V CONN'S SUPPLY 3,9
----- DENOTES 110V CONN.S. SUPPLY PINS 3,5

D23 D46 INCL ARE REVERSED FOR -Ve OPERATION

SCHEDULE 5S26851
P.C. BOARD 5B26852

INTEGRATED CIRCUIT			
IC REF	TYPE	VDD	VSS
IC1	MC1456P	—	—
IC8	MC14011	14	7
IC9	MC14013	14	7
IC12 13 14 17 18 19	MC14051	16	8
IC-	MC14066	14	7
IC7	MC14520	16	8
IC15 16	MC14526	16	8
IC5 11	MC14538	16	8
IC6	MC14556	16	8
IC20 25 INCL	LM324	4 VA+	11 VA-
IC2,3	TL084 ACN	-	-
IC10	MC14093	14	7

1	11-1-80	CHANGE TO CONNECTIONS	

RANK STRAND ELECTRIC
A DIVISION OF RANK AUDIO VISUAL LIMITED

TOLERANCES		SCALE	-	DATE
IMPERIAL	METRIC	DRAWN	L.HAYWARD	11-1-80
FRACTION ± 1/64"	1 DEC PLACE ± 0·4mm	CHECKED		11-1-80
DECIMAL ± .005"	2 DEC PLACE ± 0·1mm	APPROVED	D.ALLEN	11/1/80
ANGULAR ± 0·25°		MATERIAL -		
UNLESS OTHERWISE STATED		FINISH -		
USED ON - 1L26980				

DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

TITLE - MUX / DEMUX CARD CIRCUIT DIAGRAM

PCB 849/3

REF1828/A1
REF1828/B1
REF1828/A2
REF1828/B2

ISSUE D | DWG. N° 6A26850

DWG. Nº 6A28128 | ISSUE 7

SHT 1

INTEGRATED CIRCUITS

REF	TYPE	VCC	GND	+15V	-15V
IC7	SN74LS04N	14	7	-	-
IC22	SN74LS10N	14	7	-	-
IC5	SN74LS123N	16	8	-	-
IC4	SN74LS136N	14	7	-	-
IC10	SN74LS42N	16	8	-	-
IC1	SN74LS1BP	8	4	-	-
IC24,26	MC1413P	-	8	-	-
IC3	MC14051BCP	16	8	-	-
IC11 12 16 17	MC14066BCP Quad	14	7	-	-
IC32,33	MC14099BCP	16	8	-	-
IC27,28	MC14538BCP	16	8	-	-
IC29	MC14013BCP	14	7	-	-
IC35	MC1456P	-	-	7	4
IC6	LM311P	-	-	8	4
IC1,23,24	LM339N	-	-	-	-
IC3,6,13	LM324N	-	-	4	11
IC22,20,29	TL084ACN	-	-	4	11
IC9	MC6808P9	-	-	-	-
IC15,19	MC6821	2	-	-	-
IC14	2764-4	28	14	-	-
IC18	HM6116LP-4 12-Vnot	17	-	-	-
D15 1	DI 2416	5	2	-	-
IC37	MC14584BCP	14	7	-	-

MC9 TEST PORT PL1

IC9 6809 MPU

IC14 2764

IC18 6116

IC10 LS42

IC5 400nS

PROM DELAY LK3

RESET SW50

E000-FFFF

8000-9FFF

6000-7FFF

0000-1FFF

4000-5FFF PIA1

IC15 6821

IC19 6821

DIS1

IC25 4099

IC32 4099

IC33 4099

IC34 4051

RN9 13x680R

RN10 13x680R

RN11 6x47K

D97-99 NOT NORMALLY FITTED

SW1 SEL A · SW2 SEL B · SW3 SEL C · SW4 SEL D · SW5 SEL E · SW6 SEL F · SW7 SEL G · SW8 SEL H

SW9 C/P LOAD · SW10 Spare 1 · SW11 Spare 2 · SW12 Spare 3 · SW13 Spare 4 · SW14 NEXT DIR

SW15 1 · SW16 2 · SW17 3 · SW18 4 · SW19 5 · SW20 6 · SW21 7 · SW22 8 · SW23 9 · SW24 0

SW25 > · SW26 < · SW27 + · SW28 - · SW29 +1 · SW30 CL · SW31 + · SW32 - · SW33 1 · SW34 2 · SW35 3 · SW36 0 · SW37 . · SW38 REV · SW39 SWEEP · SW40 SHADOW · SW41 FILL

SW20

SCHEDULE SS 28129
PC BOARD SS 28130

CHASE A-H
O/Ps A-H
CHASE RATE
SYNC PULSE
SYSTEM FRAME PULSE
LOCAL FRAME SYNC
CHANNEL ON

LDATA from Test-Tool geht als CS0 an die PIA's, damit sie in HI-Imp sind, wenn Test-Bar angeschlossen, weil sie direkt am D-Bus hängen und nicht extra gebuffert sind

REVI	DESCRIPTION	BY	DATE
A	ADDED R.C. TO RESET LINE		
B	ADDED R.C. TO RESET LINE		
C	ADDED R.C. TO RESET LINE		
D	ADDED R.C. TO RESET LINE		
E	ADDED R.C. TO RESET LINE		
F	ADDED R.C. TO RESET LINE		

RANK STRAND ELECTRIC
A DIVISION OF RANK AUDIO VISUAL LIMITED

DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION

TOLERANCES: IMPERIAL — METRIC; FRACTION ± 1/64" 31 DEC PLACE ± 0.4 mm; DECIMAL ± .005" 2 DEC PLACE ± 0.1 mm; ANGULAR ± 0.25°; UNLESS OTHERWISE STATED

USED ON -
1L26980

SCALE — 1 DATE
DRAWN
CHECKED
APPROVED
MATERIAL -
FINISH -

TITLE -
M24 EFFECTS PROCESSOR PCB

PCB B73'3 REF1857

ISSUE 7E | DWG. Nº 6A28128 SHT1

DRG. No.
7C 28189
SH. OF
ISSUE AB
REV. 1. C.No. E6019 Red/Black wire Colours swapped ARR 17/8/83

IEC FILTER PLUG

MAINS INPUT 220-240Vac OR 110-120Vac 50-60 Hz

L Bn F1 2A TB1 1 120V T1 17.5V T1

E Gn/Y Bn 2 0V T2

3 120V 17.5V

N Bu F2 2A 4 0V T3

(TWIN PHASE OPTION)

EARTH STUD

220 / 240V WIRING

C1 3300µF 40V

PSU BOARD REF 1863

PL1 -15V 0V +5V +15V

6 5 4 3 2 1

BK Gn Pk R

T4 T3 T2 T1

T5

Gn/Y

F1 3,15A TB1 1 120V T1 17.5V

Bn 2 0V 0V

3 120V 17.5V

Bu 4 0V 0V

110V OPTION

WIRE SIZES

0,75 mm²

1,0 mm²

1,5 mm²

2 CORE 7/0,2 mm² O/ALL SCREENED

AUDIO I/P

1 LEFT
2 0V
3
4 RIGHT
5

SK1

M24 EFFECTS PROCESSOR BOARD REF 1857

PL2

1 FX+FADER MUX
2 0V
3 0V
4 MUX I/P
5 -
6 + SYNC

MULTIPLEX X-CON PLUG

1 3 2 Bu R Gn

(FROM MEMORY SYSTEM)

PL3

OV 1
0/P MUX 2
FADER MUX 3
2 4 WIRE 4

(2 WIRE MUX)

Bu R

MULTIPLEX X-CON SOCKET

(TO DIMMERS / DIMMER I/F)

(4 WIRE MUX)

0V 1
DMUX 2
SYNC + 3
- 4

PL4

NOTE : JUMPER PIN 4 TO 0V FOR 4 WIRE MUX OPERATION

PL1

1 2 3 ... 49 50

MC9 TEST PORT

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This Drawing shall not be copied or reproduced in any manner without the prior approval of Rank Strand Ltd.

		DATE
DRAWN	RDKirathy	9.3.83
CHECK'D		6-3-83
APPR'D		10.3.83

Rank Strand Ltd

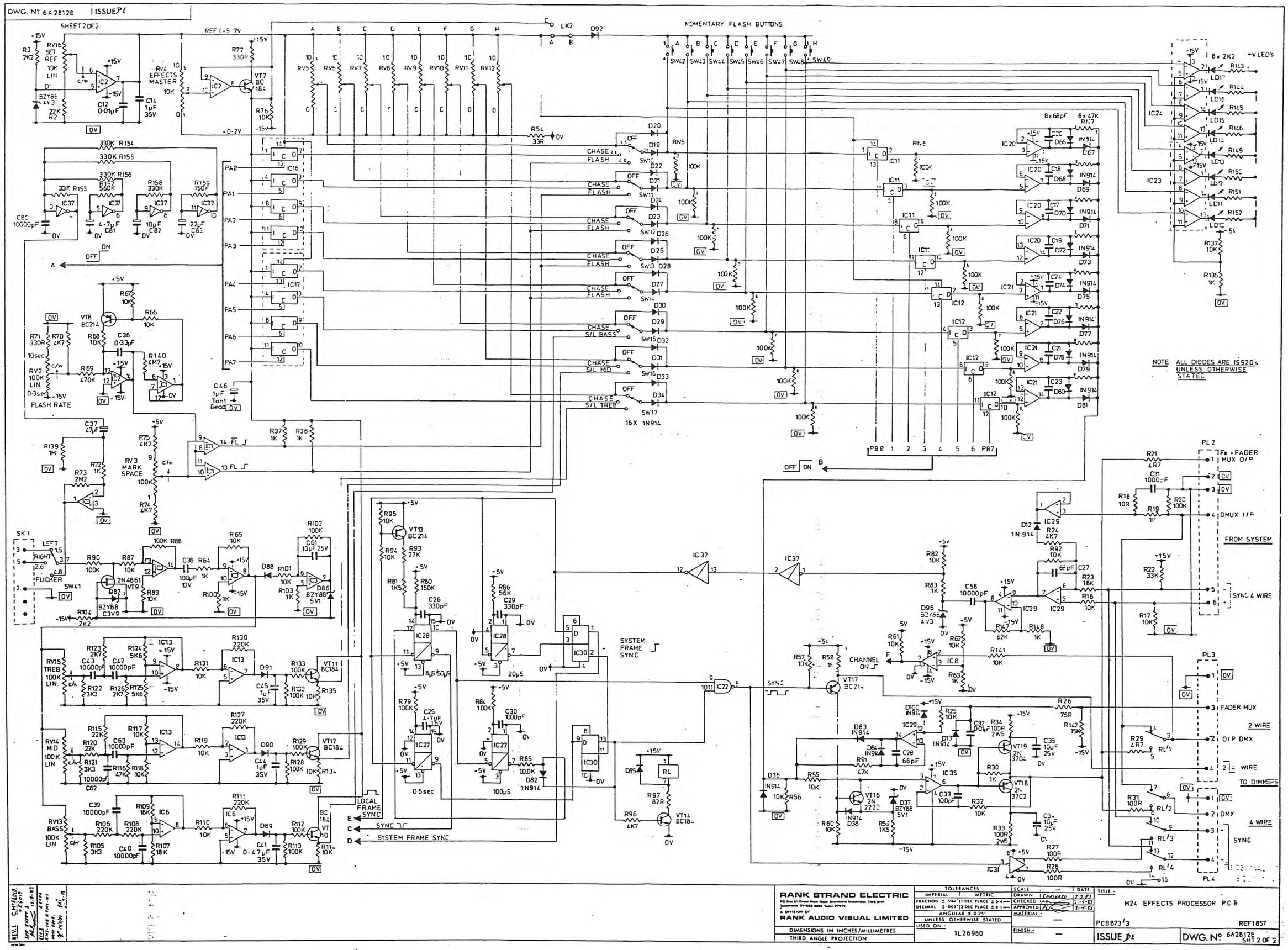
Head Office: PO Box 51, Gt. West Rd., Brentford, Midd'x. TW8 9HR
Telephone 01 568 9222 Telex 27976
Factory: Mitchelston Industrial Estate, Kirkcaldy, Fife, KY1 3LY
Telephone 0592 52333 Telex 72300

SCALE	
DIMENSIONS IN mm	
PROJECTION	
TOLERANCES	
1 DEC PLACE	±0.4mm
2 DEC PLACES	±0.1mm
ANGULAR	±0.25°
UNLESS OTHERWISE STATED	
MATERIAL:	
FINISH:	
FIRST USED ON: 1L26980 M24 EFFECTS	

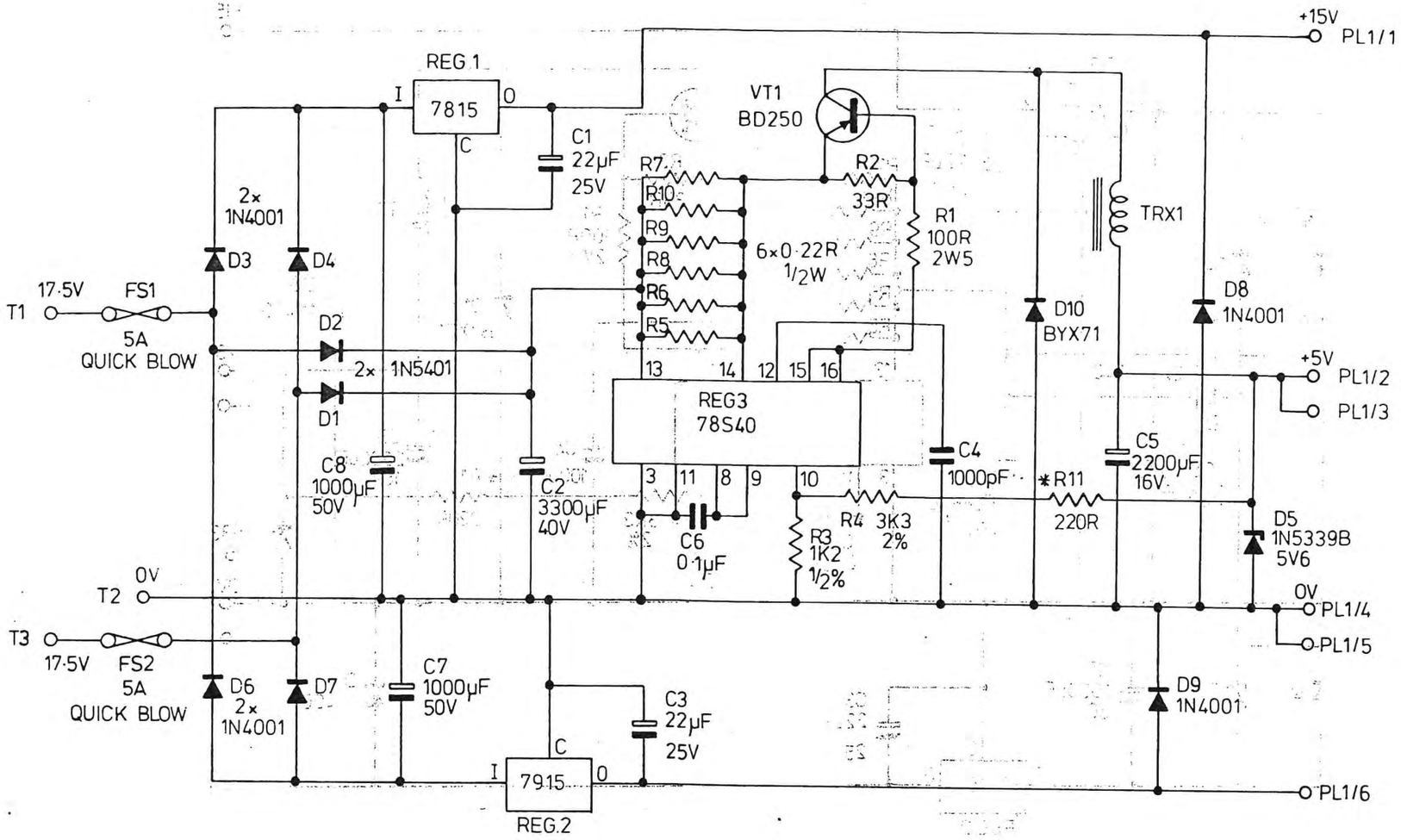
TITLE: TEMPUS M24 EFFECTS WIRING DIAGRAM.

ISSUE	DRG. No.	SH.
AB.	7C 28189	OF

H&T PDS 9


DWG. Nº 6A28128
ISSUE
SHEET 2 OF 2
MOMENTARY FLASH BUTTONS
NOTE ALL DIODES ARE IS920's UNLESS OTHERWISE STATED
FLASH RATE
SYSTEM FRAME SYNC
LOCAL FRAME SYNC
CHANNEL ON
FROM SYSTEM
SYNC 4 WIRE
FADER MUX
2 WIRE
O/P DMX
4 WIRE
TO DIMMERS
DMX
SYNC
RANK STRAND ELECTRIC
A DIVISION OF
RANK AUDIO VISUAL LIMITED
DIMENSIONS IN INCHES/MILLIMETRES
THIRD ANGLE PROJECTION
TOLERANCES
IMPERIAL
METRIC
ANGULAR ± 0.25°
UNLESS OTHERWISE STATED
USED ON
1L26980
SCALE
DRAWN
CHECKED
APPROVED
MATERIAL
FINISH
TITLE
M24 EFFECTS PROCESSOR PCB
PCB873/3
REF1857
ISSUE
DWG. Nº 6A2812E
SHT 2 OF 2

DWG. Nº 6C28178 | ISSUE A



*NOTE. RESELECT ON TEST IF O/P VOLTAGE IS OUTSIDE 4·9V–5·1V RATIO IS 1mV = 1 Ω

P.C.BOARD - 5B26866.
SCHEDULE - 5S28177

REV. 1. C.Nº	RANK STRAND ELECTRIC P.O. Box 51 Great West Road, Brentford, Middlesex TW8 9HR Telephone 01-568 9222 Telex 27976 A DIVISION OF RANK AUDIO VISUAL LIMITED	TOLERANCES IMPERIAL / METRIC FRACTION ± 1/64" / 1 DEC PLACE ± 0·4 mm DECIMAL ± ·005" / 2 DEC PLACE ± 0·1 mm ANGULAR ± 0·25° UNLESS OTHERWISE STATED	SCALE DRAWN CHECKED APPROVED MATERIAL :-		DATE 25.2.83 10-3-83 10-3-83	TITLE :- M24 EFFECTS POWER SUPPLY BOARD.
	DIMENSIONS IN INCHES/MILLIMETRES THIRD ANGLE PROJECTION	USED ON :- 1L26980 M24 EFFECTS	FINISH :-			PCB 850/3 REF. 1863
					ISSUE A	DWG. Nº 6C 28178

WW 289